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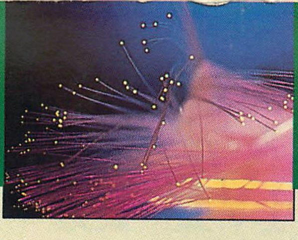

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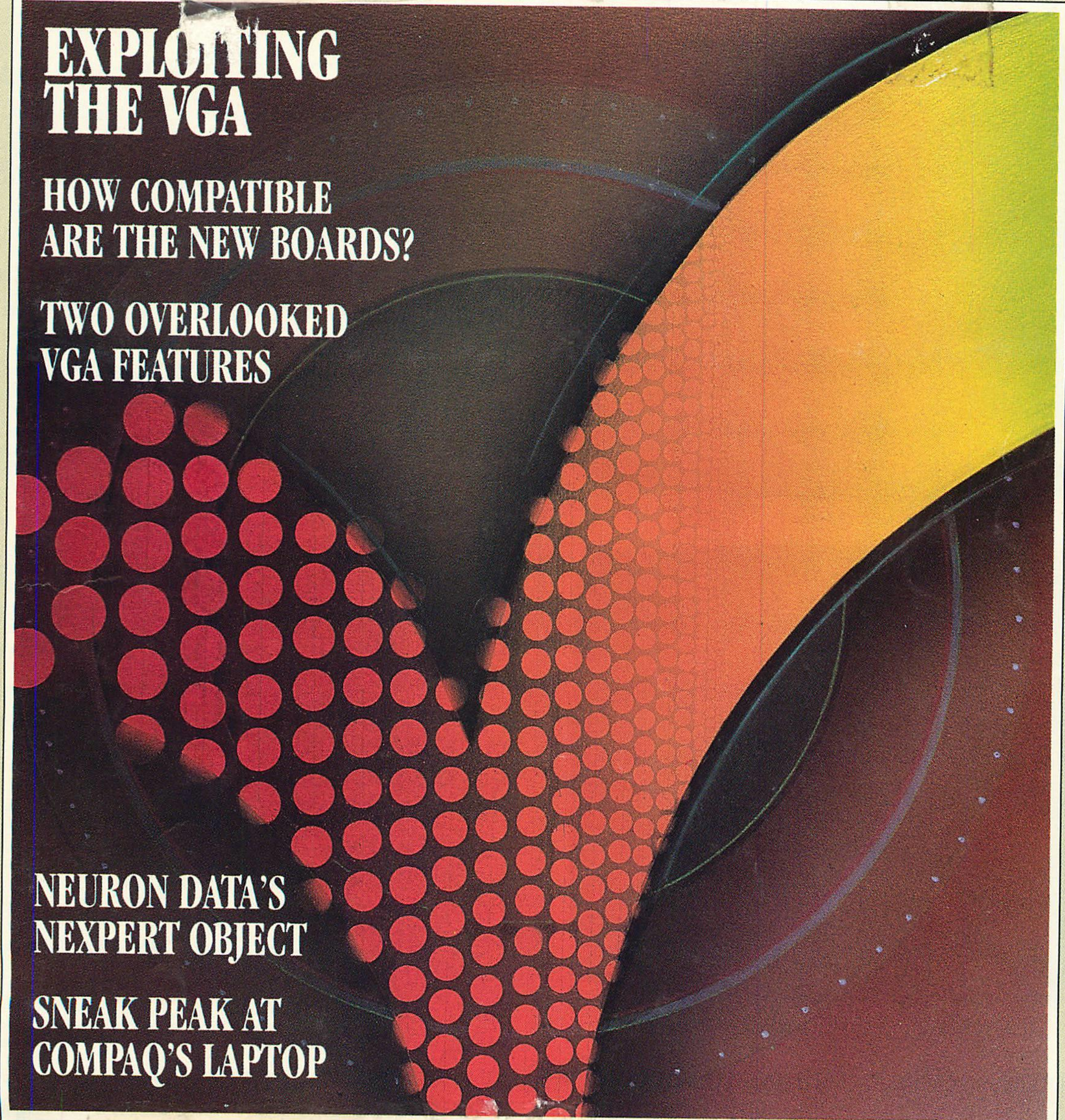
NOVEMBER 1988

VOL. 6 NO. 11 $3.95

PC TECH JOURNAL®

FOR SYSTEMS DEVELOPERS AND INTEGRATORS



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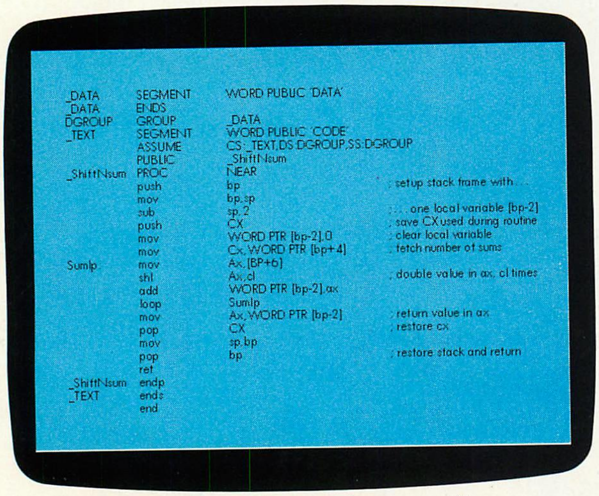
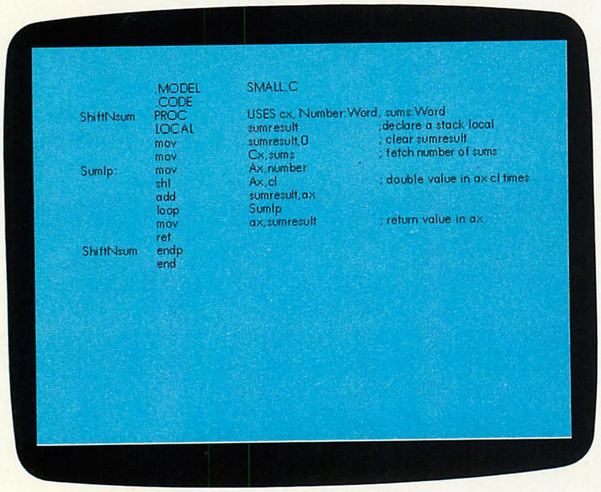


The old way: slow, cumbersome coding.



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For the details, check the techbox. For more information, call (800) 541-1261, Dept. I17. And learn how today's new Microsoft MASM is so fast and easy it comes with the following offer.

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- Comprehensive instruction set *reference* with examples.
- Programmer's Guide – complete guide to MASM features and instruction set.

Macro Assembler for MS OS/2 and MS-DOS
- Full MS OS/2 support to break the 640K barrier. NEW!
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- Assembles 25-40% faster than MASM 4.0.
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- Interactively view structures and chase linked lists. NEW!
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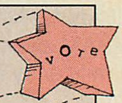
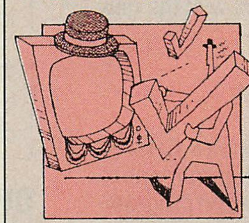
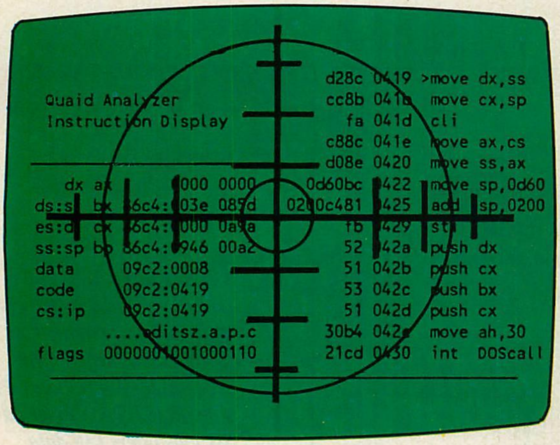
WE'RE LOOKING FOR A FEW GOOD PRODUCTS





It's an election year—time to elect a president, congress, county commissions, city councils, hardware, and software. In appreciation of the electoral process, *PC Tech Journal* asks its readers to cast their votes for the products that have served them best. Your ballot is this month's Reader Opinion Card, bound in between pages 8 and 9. This is one election in which substance will count more than charisma. Qualified candidates are those products that thoroughly understand the issues of the task before them. The winners and their backers will be duly honored in a future issue. Don't forget to vote.

Cover illustration · Andy Levine



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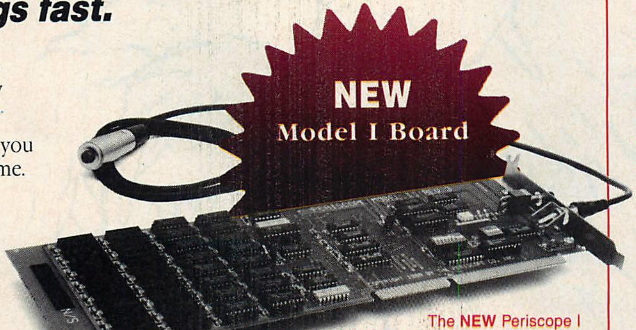
Periscope's *New* Version 4

...Gives you all the right stuff for debugging! No matter which model you pick, you have the same powerful software to help you track down hard-to-find bugs fast.

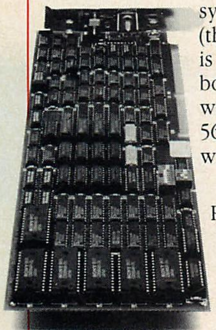
Periscope's hardware adds the power to solve the really tough debugging problems.

The break-out switch lets you break into the system any time. You can track down a bug instantly, or just check what's going on, without having to reboot or power down and back up. That's really useful when your system hangs! The switch is included with Periscope I, Periscope II, and Periscope III.



The **NEW** Periscope I memory board keeps all debugging information out of the lower 640K. Can be used in PCs, ATs, and 386s with both EGA/VGA and EMS boards installed. The Periscope break-out switch enables you to recover from a hung system. Included with Models I, II, and III.

Periscope I has a **NEW** board with 512K of write-protected RAM, user-expandable to 1MB, for the Periscope software, symbol tables, and all related debugging information. Normal DOS memory (the lower 640K) is thus totally freed up for your application, and Periscope is protected from being overwritten by a run-away program. The new board's footprint is only 32K, so you can use it in PC, AT, and 386 systems with EGA/VGA and EMS boards installed (not possible with the previous 56K board). It can also be used with Periscope III to provide additional write-protected memory.



Periscope III has a board with 64K of write-protected RAM to store the Periscope software and as much additional information as will fit. AND...

The Periscope III board adds another powerful dimension to your debugging. Its hardware breakpoints and real-time trace buffer let you track down bugs that a software-oriented debugger would take too long to find, or can't find at all!

The Periscope III hardware-breakpoint board captures information in real-time, so you'll find bugs that can't be found with a software-based debugger.

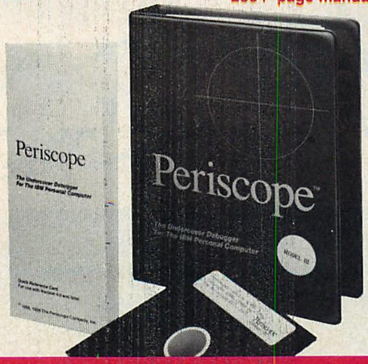
Periscope's software is solid, comprehensive, and flexible.

It helps you debug just about any kind of program you can write... thoroughly and efficiently.

Periscope's the answer for debugging device-drivers, memory-resident, non-DOS, and interrupt-driven programs. Periscope works with any language, and provides source and/or symbol support for programs written in high-level languages and assembler.

David Nanian, President of Underware, Inc. (of BRIEF fame) says this about the new Periscope Version 4:

"Periscope has always been an unbelievable assembler-level debugger. Version 4 has turned it into a terrific source-level debugger as well. Aside from major enhancements like the source-level improvements, all the little changes make a really big difference, too. For instance, symbol lookups and disassemblies are noticeably faster, and highlighting the registers that have changed really makes life easier. Once again, Periscope has raised the industry standard for debuggers!"



Periscope software & 250+ page manual

What's New in Periscope Version 4:

- View local symbols from Microsoft C (Version 5)
- Debug Microsoft windows applications
- Set breakpoints in PLINK overlays
- Improved source-level support
- Monitor variables in a Watch window
- 80386 debug register support
- Debug using a dumb terminal
- PS/2 watchdog timer support
- Use mixed-case symbols
- Set breakpoints on values of Flags
- Much more!

- **Periscope I** includes a **NEW** full-length board with 512K of write-protected RAM; (user-expandable to 1MB); break-out switch; software and manual for $695.
- **Periscope II** includes break-out switch; software and manual for $175.
- **Periscope II-X** includes software and manual (no hardware) for $145.
- **Periscope III** includes a full-length board with 64K of write-protected RAM, hardware breakpoints and real-time trace buffer; break-out switch; software and manual. Periscope III for machines running up to 10 MHz with one wait-state is $1395.

Due to the volatility of RAM costs, prices on board models are subject to change without notice.

REQUIREMENTS: IBM PC, XT, AT, PS/2, 80386 or close compatible (Periscope III requires hardware as well as software compatibility, thus will not work on PS/2 or 80386 systems); DOS 2.0 or later; 64K available memory (128K at installation time); one disk drive; an 80-column monitor.

Call us with your questions. We'll be happy to send you free information or help you decide on the model that best fits your needs.

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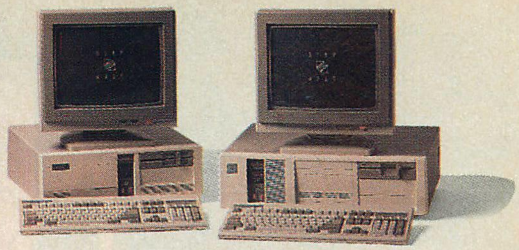
Step 286/20	4.24 MIPS
Step 386/20	4.91 MIPS
Step 386/25	6.13 MIPS

Source: Power Meter MIPS Version 1.3. The Database Group, Inc.



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SYSTEMS PERSPECTIVE

Dangerous Dependencies

A missed product-release date compromises developers who depend on that product for their applications. □ Also, VGA compatibility.

Like fine wine, software should not be released before its time. I realize complex software cannot be written quickly. It takes time to design, code, alpha test, beta test, and gamma test. So, I'm willing to wait a prescribed period of time for the release of preannounced software.

I believe in preannouncements, too—as long as vendors keep their promises. Preannouncements are beneficial to both the customer and the vendor. The customer is able to develop strategic plans based upon tools that will be available at a later, predictable date, and the vendor stalls the customer—keeping him or her from buying a competitor's product by promising superior features, thereby assuring a market for the product once it is finally released.

The danger is that by missing preannounced dates, the vendor puts the developer at his mercy. If the product is an upgrade to an existing tool, for example, the developer already has a substantial investment in customized applications he has written using this tool and in end users trained in the operation of these applications.

This problem is even more pronounced with tools that are built for the horizontal market, such as spreadsheets, communications software, and data managers that have a proprietary internal language and provide a ready-made interface that the developer can pass on to the end user.

Creating applications with these packages is tempting to the developer because of the shorter development cycle. The developer, however, may become unhealthily dependent on a vendor, with no control over when the next version will be released or what features it will contain. In effect, when the vendor misses a delivery date, the developer's application is stalled, waiting for the features needed to move the application forward.

The developer could turn to a competitive product. Other vendors, also having heard the preannouncement, are sure to try—and often succeed—at beating the preannouncing vendor to the market. The vendors enter a race to the finish, each trying to pack the best features into the first available product. Choosing the competitive product, however, means the developer must absorb the costs of buying the new package, rewriting the application in a new proprietary language, and retraining the end user before seeing any new benefits.

A prime example is the delay of version 3.0 of Lotus 1-2-3 from an originally announced June shipping date. Two competitors, Microsoft and Borland, have released excellent spreadsheets (Excel and Quattro, respectively) bearing features not available in the current version of 1-2-3. Still, many of 1-2-3's seven million users are waiting rather than switching.

Even though both Excel and Quattro read 1-2-3 spreadsheets and interpret 1-2-3 macros, and Excel's help files explain the operational differences between 1-2-3 and Excel, the conversion costs both time and money, while upgrading to Lotus 1-2-3 version 3.0 is minimal cost. Additionally, developers need to learn the custom language of Excel or Quattro to enhance the application after it is converted.

A single-source language is anathema to the developer. The saving grace for Ashton-Tate's dBASE IV, also delayed, is that its language is supported by many sources. Converting from dBASE to one of its dialects is no more difficult than converting from one C compiler to another.

MISSING DEADLINES

Vendors cannot or do not meet their deadlines for several reasons. Most preannounce their products too early in the development cycle without first determining whether or not they can deliver the alleged features by the target date. This leads to unrealistic development timetables.

Some schedules are put aside because midway through development, a competitor releases or announces a product with features not originally scheduled in the vendor's product. The vendor often decides to add these features even though it means missing the target release date.

Revising the features list is understandable before the product is announced. Once the announcement is made, however, the vendor owes it to

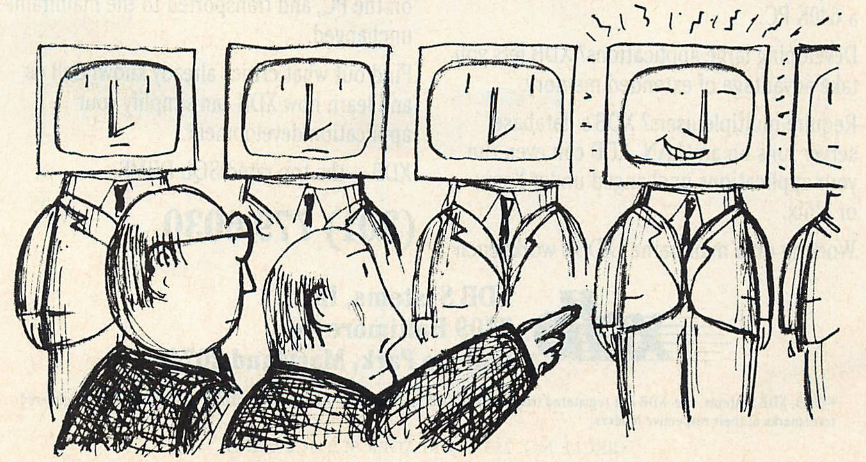


ILLUSTRATION • MACIEK ALBRECHT

his loyal and captive customers to release the product on time. These customers are not going to jump ship if treated with consideration, and new features can always be added to the next release.

The vendor also owes it to developers to provide an open system with a hook for integrating code from other sources. This unties developers' hands, thus allowing them to add features—whether or not the vendor delivers the product on schedule.

VARIATIONS ON A VGA THEME

Magazines know better than anyone about the consequences of missed deadlines. We, therefore, have produced this month's issue in as timely and thorough a manner as possible to bring you up to date on the latest graphics standard.

Although the PS/2 has not been the runaway success IBM had hoped, one of its features, the VGA, has been warmly embraced by the entire industry. Many computer vendors are integrating VGAs onto their system boards, and every major graphics board manufacturer has produced a VGA adapter for classic-bus machines.

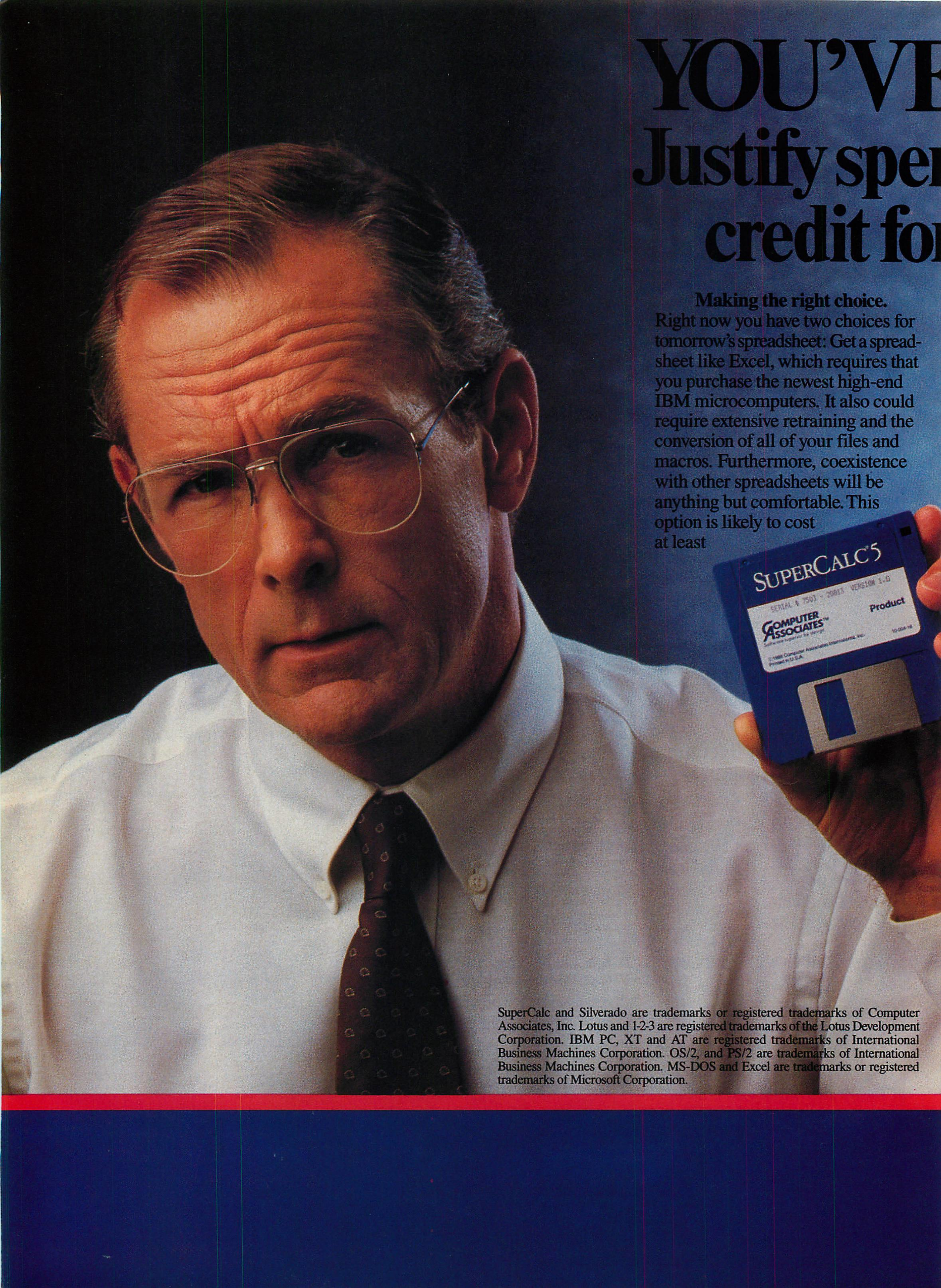
As with any de facto standard, variations abound. In the first article in our cover suite ("The VGA Compatibility Test," p. 48), Ed McNierney and Kent Quirk define what VGA compatibility means and present a test program that determines how a VGA implementation measures up to the standard. Code for this metric is available for downloading on PCTECHline, 301/740-8383.

In the second article ("Pixel Panning and Split Screens," p. 62), Richard Wilton explains how to use the VGA's panning feature to scroll through data in the video buffer.

Finally, in Tech Notebook (p. 143), Arun Johary and Bo Ericsson of Chips & Technologies reveal to technical editor Ted Mirecki an undocumented feature of the VGA that allows developers to pack five times the normal number of characters on the screen.

WE WANT YOUR VOTE

In the spirit of politics and elections, *PC Tech Journal* is giving its readers the opportunity to vote for their most prized products on this month's Reader Opinion Card, which is bound in on the previous page. We will be looking for your best explanations about how a product has made your life easier. Vote now and watch for election results in the February issue.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Making the right choice.
Right now you have two choices for tomorrow's spreadsheet: Get a spreadsheet like Excel, which requires that you purchase the newest high-end IBM microcomputers. It also could require extensive retraining and the conversion of all of your files and macros. Furthermore, coexistence with other spreadsheets will be anything but comfortable. This option is likely to cost at least
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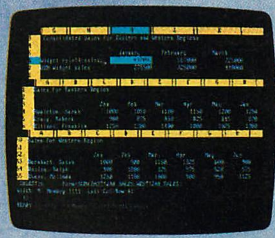
Introducing SuperCalc®5.
Tomorrow comes in a blue and red box. *SuperCalc5* is the spreadsheet of the future, ready for you today. First of all, it works with the hardware you most likely have on your desk right now, including all IBM PC,® XT,® AT® and PS/2™ models and compatibles with 512k memory. *SuperCalc5* has been designed for MS-DOS and to bridge the migration to OS/2. It also supports LIM version 4.0 providing up to 32 mb of memory.

In use, *SuperCalc5* holds up to 255 spreadsheets in memory and allows you to view and manipulate any three of them on screen at any one time. Direct links can be established with spreadsheet files in memory, on disk or on a network. And these can be a combination of *SuperCalc* and Lotus 1-2-3® files. There's even a version for your company mainframe called *CA-SuperCalc.®*

SuperCalc5 was designed to coexist with Lotus 1-2-3. Not only does it read, write and link to 1-2-3 files automatically, *SuperCalc5* includes an optional 1-2-3 menu and can use 1-2-3 macros. You can even move Lotus 1-2-3 macros into *SuperCalc5* and then back again.



Accuracy and speed.
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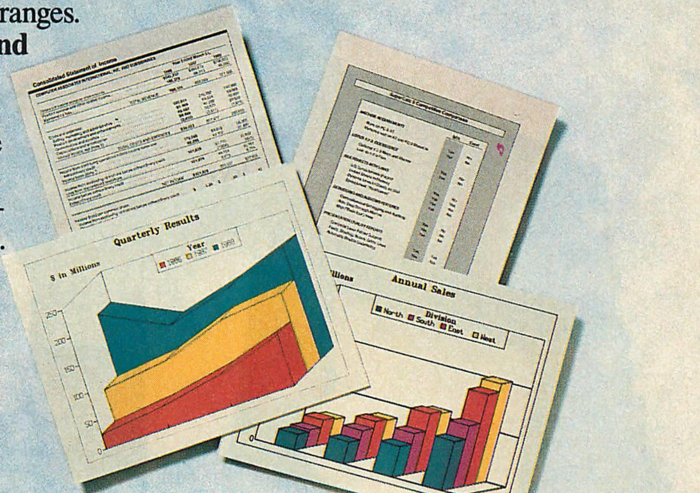

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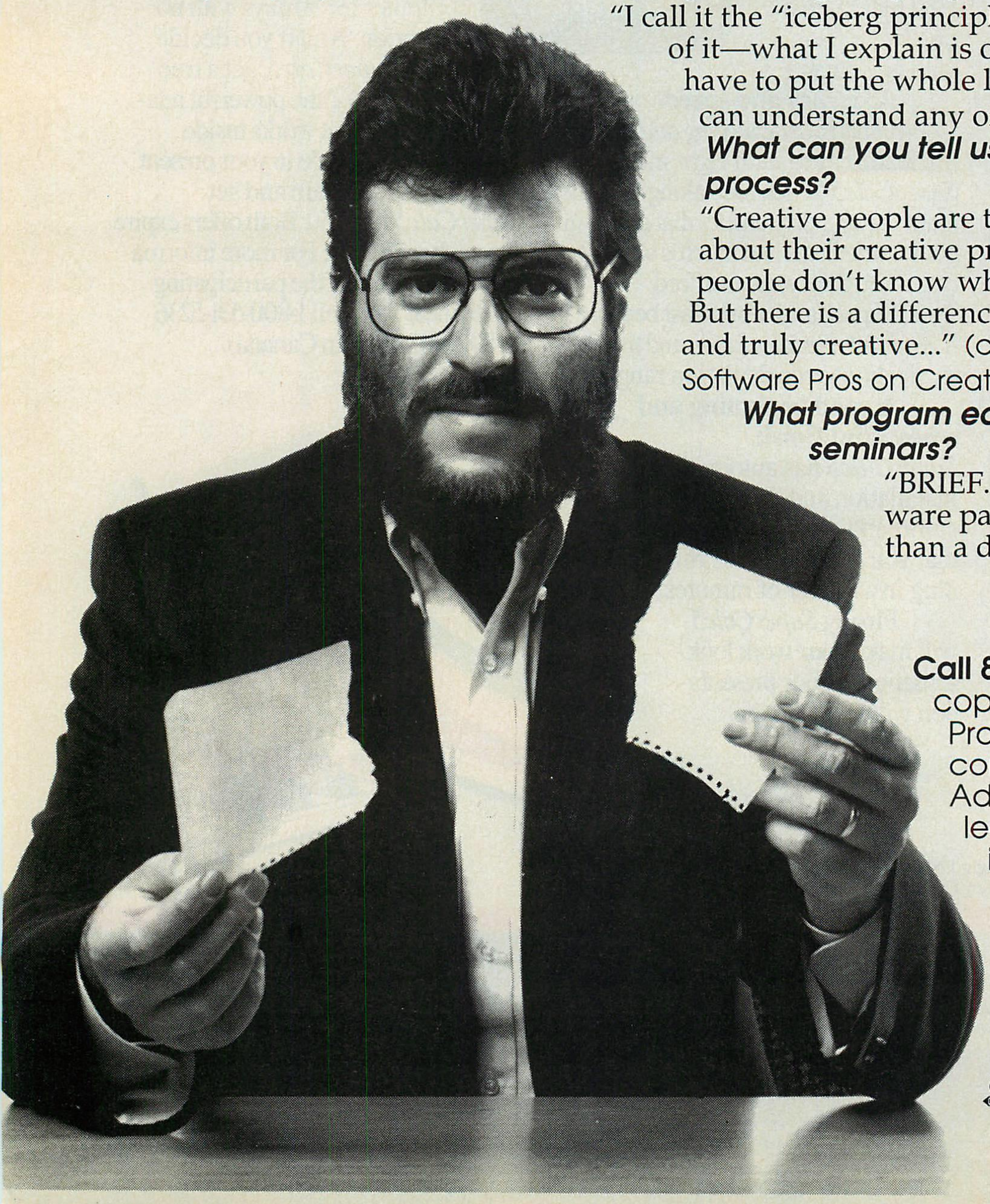

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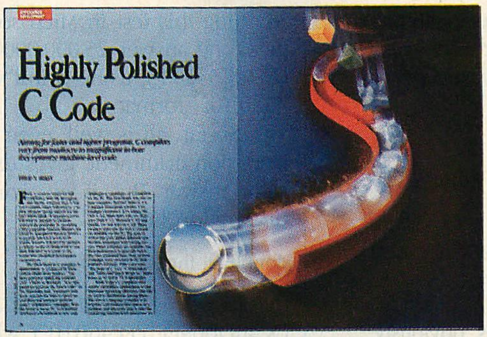
LETTERS



Highly Polished C Code

New Directions

Analyzing the Apple Suit

ROUGH AROUND THE EDGES

While I really appreciated the information imparted in the article "Highly Polished C Code" (Philip N. Hisley, June 1988, p. 76), I feel I must make one important point: no amount of optimization can make up for incorrect code generation.

Attached is a printout of a section of code we attempted to use and the resulting assembly code generated by Manx Software Systems' Aztec C compiler. Close inspection reveals that the output code incorrectly skips every other byte. We wasted several weeks tracking down this type of problem in a ROM-based toll-collection terminal we were developing.

"Highly polished" would not necessarily be my choice of words to describe much of the existing offerings.

Larry R. Waibel
Ramona, CA

The code example that Mr. Waibel provided is too large to reproduce here in its entirety; a program demonstrating the bug is shown below:

```
main()
{
    char src[2], dst[2];
    int i = 0, j = 0;
    dst[j++] = src[i++] & 0x0F;
    printf("Variable j is %d\n", j);
    exit(0);
}
```

When this program is compiled and run with Aztec C 4.1C, the value of j is 2, rather than the correct value of 1. Inspection of the generated assembly-language code reveals that the compiler had incremented j twice in the code for the assignment statement.

I contacted the Aztec support staff at Manx Software Systems Inc. through its bulletin board (201/542-2793) and left a copy of the above program. Within a week, they sent me a beta test copy of version 4.1D that ran the test program correctly. At this time, the release date and price of the enhanced version is not available.

—DWM

THE USER IS THE LOSER

Two items in your September 1988 issue—Will Fastie's comments on the Apple suit (New Directions, p. 23) and a letter to the editor ("Free the Data Structures," Evan P. Provisor, p. 15)—together with recent pieces of a similar vein in other PC magazines, lead me to conclude: the user is the loser.

We are treated to a rapid proliferation of bus architectures (all noncompatible) and new operating systems are mushrooming all around us, but all this attention is going into architecture and CPUs and almost none into the NPU, or non-power user. The NPU is computerdom's version of the ordinary man on the street, someone using a computer to get a job done because, hopefully, it can be done faster, better, with fewer errors and headaches.

The users (NPUs and developers alike) are not served by fragmentation and endless proliferation of new standards (particularly when each of the so-called standards is supported by only a handful of vendors). If, to avoid a lawsuit, each new system must have a different "look and feel," the user is debilitated by having to learn a different gestalt each time a new program is encountered—and worse, shift mental gears when trying to use several programs in tandem. A new program on a new machine may be many times faster than what we are currently using.

About the best that can be said for much of the software reaching the marketplace today is that it *almost* works. It may work on your particular combination of hardware, and then again, it may not. If you can get it up and running, the odds are very high that it will contain at least several bugs (or are they called anomalies?). The chances are excellent that before you have it installed, you will see advertisements for the next version.

Did you ever wonder how IBM came up with the idea for PS/2? Do you think that IBM polled consumers? Did they ask NPUs, "What would you like to see incorporated into a new system?" Was there any market research?

The user is the forgotten man. Today, the giants of the computer industry remind me of the Big Three back in the halcyon days of the American auto industry. There was no need to ask the consumer what he wanted—they *knew* what he should want. One day they woke up and found that half their business was gone.

What the NPU needs today is a champion, a white knight, a Ralph Nader—someone willing to throw down the gauntlet and challenge the giants of the computer world who are busy telling us what we need and what's good for us. Someone who can say: "Hey look, these things are unsafe at any speed."

Mark Harris, senior partner
Harris and Hall Associates
Port Angeles, WA

QB4 PRECISION EXPLAINED

I believe that the results reported for Microsoft's QuickBASIC 4.0 in single precision (Letters, C. W. Tittle, August 1988, p. 16) may be more explicable and less "astounding" than they appear. (For a review of QuickBASIC 4.0, see Product Watch, Justin Crom, May 1988, p. 149.) Many compilers and their libraries map all calls to floating-point functions to the double-precision version, which may be the only one supplied. This has benefits for the compiler developer, who has to supply only one routine, and it can hardly hurt the user, who gets more precision than he or she bargained for. However, the results of floating-point computations are sometimes not obvious.

Let's take a look specifically at the SAVAGE benchmark. Code for this test would read (in C with single precision) as follows:

```
float a; int i;
a = 1.0;
for (i = 1 ; i < 25,000; i++) {
   a = tan(atan(exp(log(sqrt( a * a )))))
   + 1.0;
}
/* the correct value of 'a' is, obviously,
   25,000 */
```

Running this test in Microsoft C 5.0 gives the answer 25,000.0000000000 (X'46C35000'), using **printf** with a '%20.10f' format.

So far, all is well; even single-precision arithmetic gives exactly the right answer. But, if we change the declaration line to:

```
double a; int i;
```

the answer is 24,999.9999972387 (X'40DB69FF FFF46B1B'), which is no longer accurate.

It seems that we have lost accuracy by switching to higher-precision arithmetic. Making the following small change to the code sheds light on what is happening:

```
float x;
double a; int i;
a = 1.0;
for ( i = 1 ; i < 25,000; i++) {
   x = tan( atan( exp( log( sqrt( a*a ))))) ;
   a = x + 1.0 ;
}
```

Now, the answer is 25,000.0000000000 (X'40DB6A00 00000000').

Small errors inevitably occur in the evaluation of functions in SAVAGE because of approximation error, round-off error, and so on. These generally affect only the low-order bits of the result. Narrowing the value to float on each iteration effectively chops off the errors; in essence, this means that the loop is counting to 25,000 by 1, which is well within the capacity of 22 to 23 bits of accuracy.

Richard E. Gibbs, CFA
Investment Cybernetics
New York, NY

If the conversion from long to short is done with an intelligent rounding algorithm, the accuracy of the reported result may seemingly improve because the rounding process can mask intermediate errors. However, a simple chopping or truncation of the bits prone to contain approximation and round-off errors may make matters worse if the intermediate errors are unequally distributed above and below the correct answer. QuickBASIC 4.0's treatment of the same code differed between the programming environment and command-line compilation, yielding different results.

—Justin Crom

TELLING THEM APART

I have a correction to Tech Notebook 82: ("Determining CPU Type," Bob Felts, November 1987, p. 51). The problem is the naming of the code segment _TEXT. This interacts badly with the Microsoft Overlay Linker delivered with Microsoft C 5.1.

The problem arises if you place CPUTYPE.OBJ in an overlay. Because it has a segment called _TEXT, all of the C runtime library gets linked into that overlay instead of into the root, including the start-up code. The resulting linked module will not execute at all. However, by renaming the segment CPUTYPE_TEXT, the problem vanishes.

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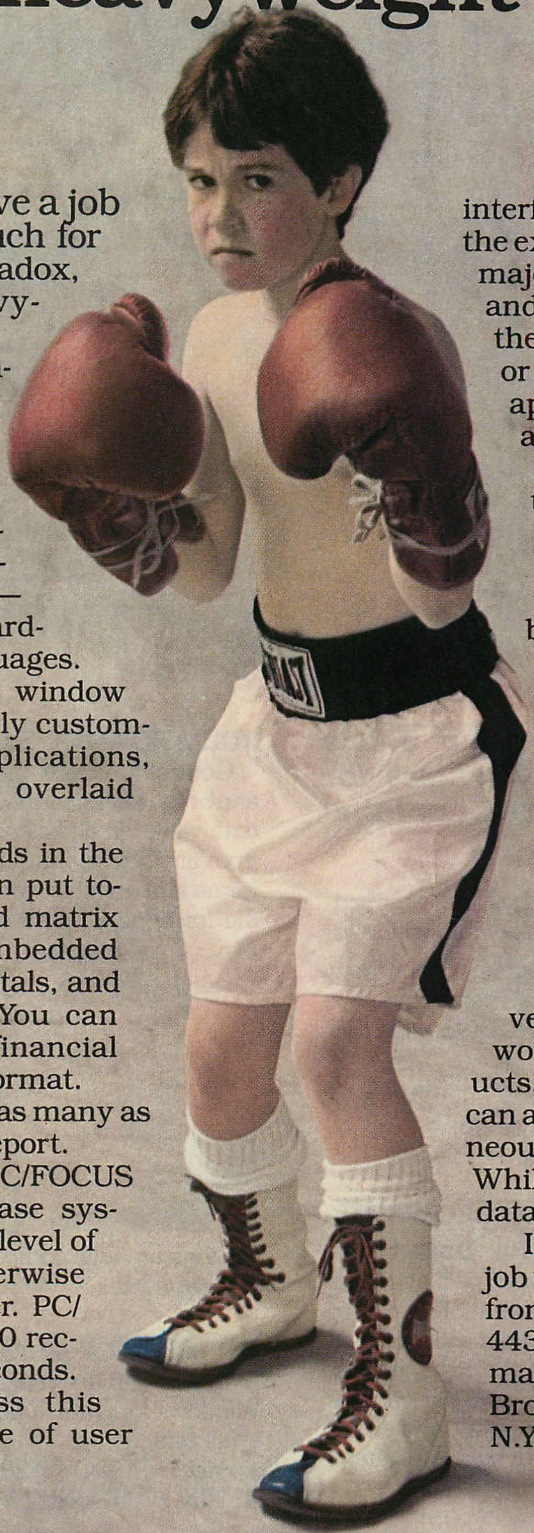

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Also, I was disappointed that the reader was referred to an earlier issue for the 8088/86 code, because I did not have access to that issue ("Chips in Transition," Bob Smith, April 1986, p. 56). I took code for detecting an 8088/86 from the other cited article ("Compatibility and Performance: Updating the Evaluation Suite," Paul Pierce and Steven Armbrust, March 1987, p. 70).

In spite of the claim in the November Tech Notebook, this code does not write into the code segment during its CPU determination, at least as far as I can detect (unless somehow the code puts the stack in code space, which is irrelevant). The code I took does not distinguish an 8088 from an 8086; if there is any way to detect the difference between the two, it would be nice to have someone publish a complete CPU-type determination. I much prefer the technique of the November issue—to return to a meaningful integer—instead of the obscure and nonsymbolic values of 1, 2, 3, and so on of the evaluation suite.

Joseph M. Newcomer
Pittsburgh, PA

As stated in the Tech Notebook article, segment naming in the CPUTYPE procedure follows the Microsoft mixed-language conventions. These conventions, which are documented in the Mixed Language Programming Guide supplied with the Microsoft assembler and compilers since version 5.0, require different names for different memory models.

Whether overlays are used or not, the published segment name is correct for the small and compact memory models, and the name used by Mr. Newcomer is correct for the medium and large models. These details were not repeated in the article because of space limitations.

Code to detect an 8088/86 was not omitted from CPUTYPE; the procedure as published does in fact detect these processors without the need for any code from the ATPERF program of the evaluation suite. ATPERF, as updated in March 1987, no longer writes to the code segment, but it does not determine the operating mode (neither real nor protected).

Again, space limitations prevented inclusion in CPUTYPE of the code to distinguish between 8088/86 processors. A complete CPU determination program, CPUID, was published in the earlier April 1986 issue. Both ATPERF and CPUID are available for downloading from PCTECHline, 301/740-8383. (Parameters: 2400/1200/300 bps, no parity, 8 data bits, 1 stop bit.)

—TM

ERRATA

In Justin Crom's reply to a letter from C. W. Tittle on QuickBASIC 4.0 (Letters, August 1988, p. 16), the second sentence of the first paragraph of the reply should read: In contrast, the .EXE file generated by the QB4 compiler from the same single-precision source code yielded the *correct* result.

Tech Notebook, September 1988, had an error in the listing on page 143 for ASKSYS.ASM. Lines 54 and 55 of the program should read as follows:

```
       int8 = 8*4
boot2: xor     ax,ax
```

In the published version, the label was inadvertently placed one line too high. We apologize for any inconvenience caused by this error. An updated listing is available on PCTECHline.

In Tech Releases in the September 1988 issue, a reader service number was omitted from the item on Herald Mail from Emissary Systems Limited (p. 38). Readers interested in this product can circle number 332 on the reader service card in the current issue. In the same Tech Releases column, the telephone number for Compaq Computer Corporation was incomplete. The number is 713/370-0670.

An incorrect telephone number was listed for CADWARE, a vendor listed in the sidebar "A Sampling of CASE Tools" in the article "The CASE for Structured Development" (Carma McClure, August 1988, p. 51). CADWARE's telephone number is 203/397-2908.

PC Tech Journal sincerely regrets these errors.

COMMENTS WELCOME

All letters to the editor should be directed to Editor, *PC Tech Journal*, Suite 800, 10480 Little Patuxent Parkway, Columbia, MD 21044. Correspondence also can be submitted over MCI Mail to PCTECH.

Although *PC Tech Journal* cannot publish all letters received, every effort is made to answer as many as possible. Please keep letters to the point; include name, mailing address, and telephone number; when a letter is lengthy, a diskette is appreciated.

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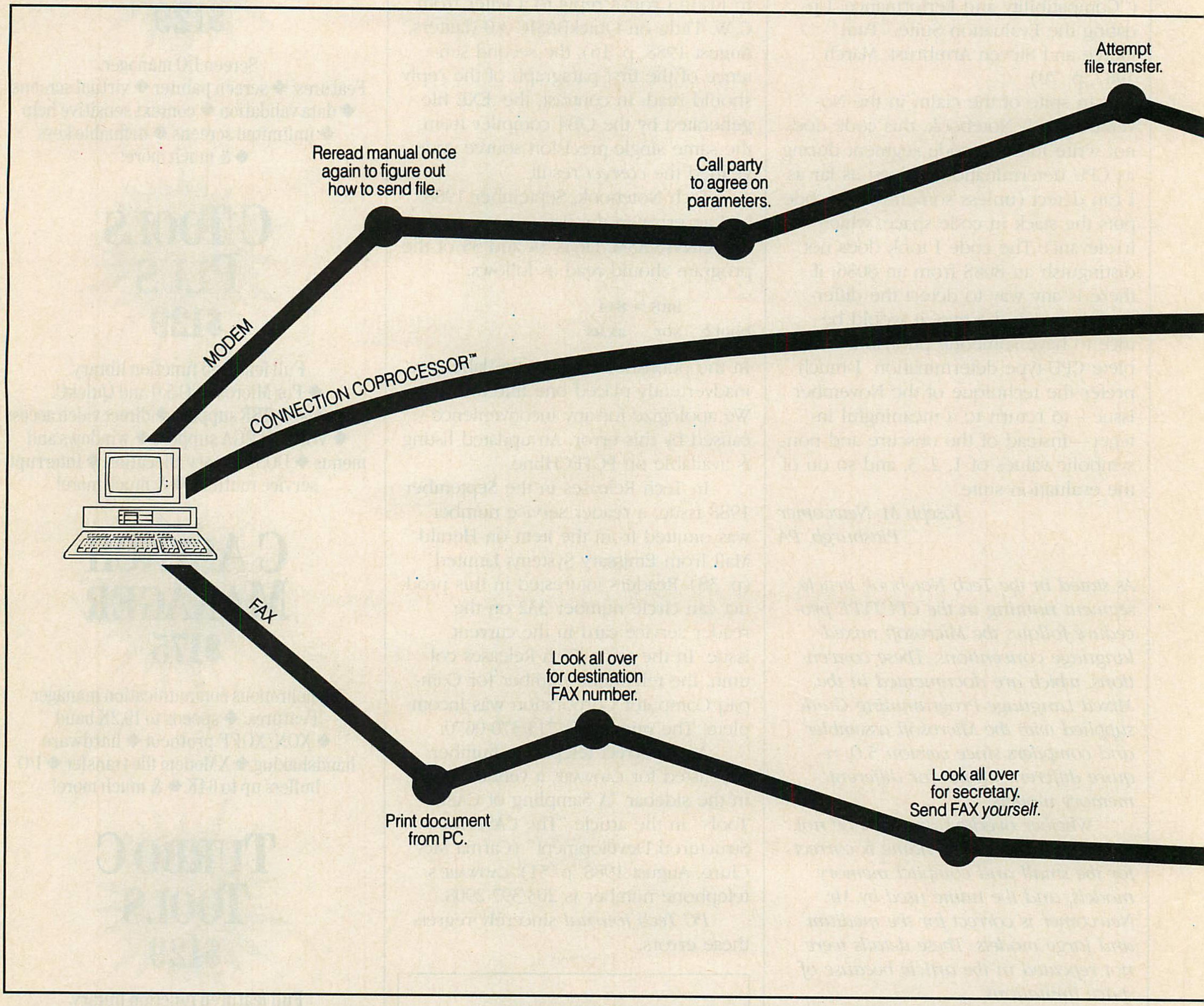

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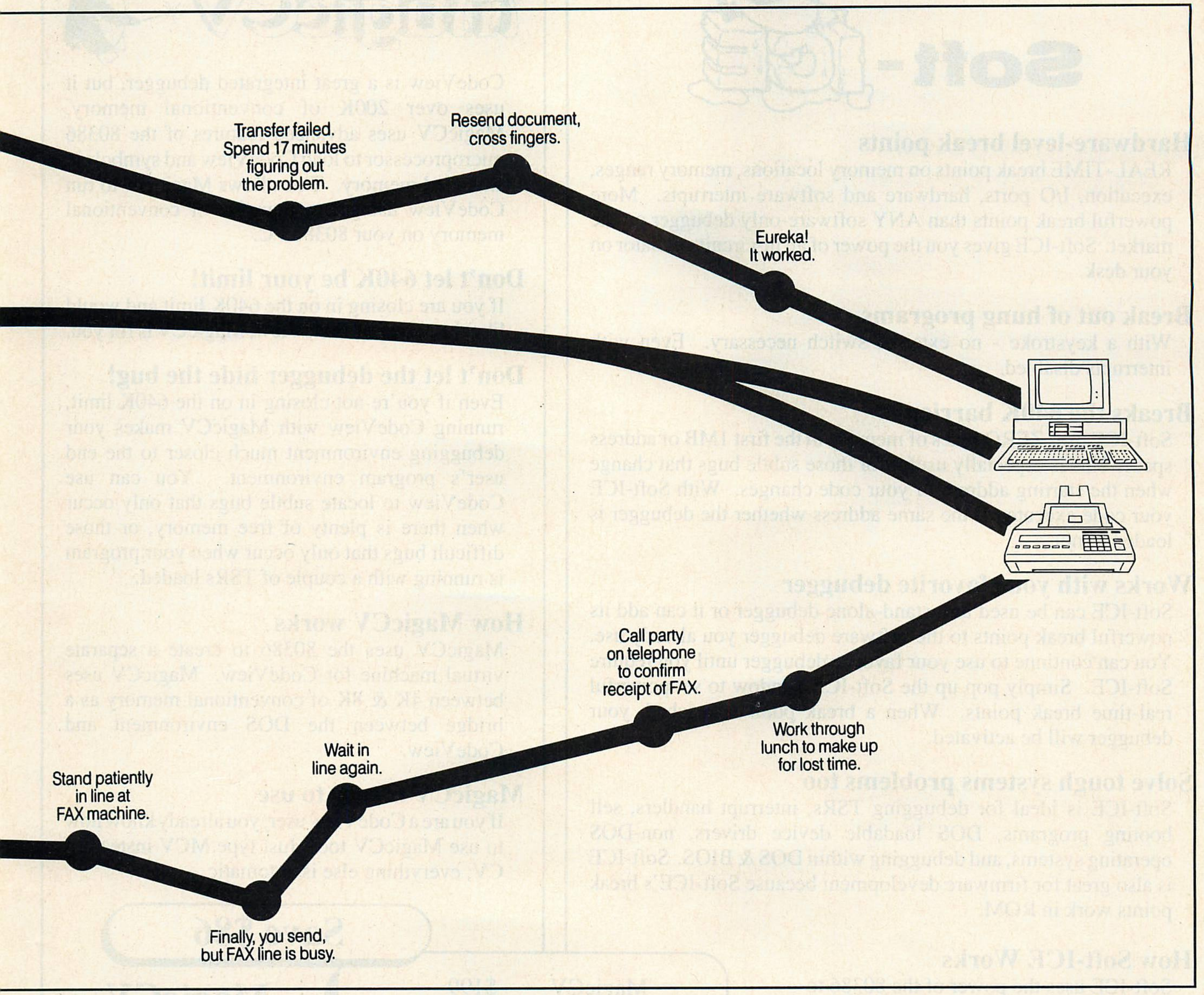

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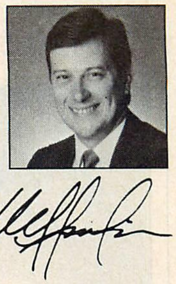

Compaq's First True Portable

With the SLT/286, Compaq moves from the realm of transportables to portables. □ *Also, new VGA technology; and MacWorld*

Compaq Computer Corporation founded its successful business on the premise that some computer users might want to carry their computers around with them. Not just any computer, mind you, but one that affords the same functionality on the road as a desktop machine. True to its origins, Compaq has made every one of its transportable computers in that same mold, allowing travelers to carry (or lug) their desktop with them.

Because portable computers are so much a part of the Compaq mystique, we all have expected for quite some time that the company would offer a true portable. By *true* I mean a clamshell design—that tiny, light, use-it-anywhere form factor that differentiates a portable from a computer-in-a-suitcase. Industry pundits have been predicting such a machine from Compaq for the last 18 months. That machine is finally here, and it's a dandy.

The 14-pound unit is called the SLT/286. The letters stand for Super LapTop; while I would prefer that Compaq leave the adjectives to those of us who make our living writing them, I am compelled to agree with their choice of words. The two features that make the SLT especially deserving of its name are its superior, VGA-compatible, backlit LCD screen and its power-conservation technology.

The SLT is a 12-MHz 80C286 (*C* for CMOS) with 640KB of standard RAM, one enhanced nicad battery, an integrated VGA display, a single 1.44MB 3.5-inch diskette drive, and either a 20MB or 40MB hard disk. The smaller hard disk has an average access time of less than 29 ms and a 3:1 interleave, while the 40MB version has the same access and a 1:1 interleave.

The standard unit also includes a parallel port, serial port, and external VGA interface, keyboard connector, and options interface. Memory can be expanded with a maximum of three 1MB modules on the system board for a system total of 3.6MB; memory can be either extended or expanded (compatible with version 3.2 of the Lotus/Intel/Microsoft expanded memory specification) with a supplied driver.

Internal options include an 80287 coprocessor, a Hayes-compatible 2,400-bps modem, and a second serial port. The modem and the second serial port occupy the same space in the SLT, so only one of those two options can be used. External options include a storage module that can house either a 1.2MB diskette drive, a 360KB diskette drive, or a 40MB tape backup unit.

Another external option, the Desktop Expansion Base, provides two classic-bus slots for, using Compaq's term, "industry-standard" expansion boards. The unit includes its own power supply, which not only powers the expansion slots but also supplies sufficient power to operate the SLT/286 and charge the battery at the same time. The Desktop Expansion Base attaches to the back of the SLT and connects via the external options interface.

While the SLT fits the definition of a clamshell configuration, it is somewhat different from its predecessors. When closed, it looks much more like a lunchbox (see photo 1) than the Compaq Portable III, which carries that nickname (see "Portable III," Jim Shields, May 1987, p. 76). Closed, the SLT's dimensions are 13.5 inches wide by 8.5 inches deep, which is reasonably compact. It is just under 4.25 inches high (or perhaps the word is thick), so it is not as flat as the typical laptop. Both the IBM Convertible and the Toshiba 1200 are 2.75 inches thick.

Quantifying the size of laptop machines is difficult because of their different shapes and structures, so I propose five measures: volume, weight, density, footprint, and lapload—a derivative of footprint coined by senior technical editor Jim Shields, our resident systems specialist. When using these measures, it is helpful to have a point of comparison, but as is typical of laptop machines, there is nothing else quite like this new model. What may come closest is the well-known 286-based Toshiba 3100 (see "Toshiba 3100," Ashley Grayson and John Vornholt, May 1987, p. 86); this comparison suffers, however, because the T3100 does not operate on batteries.

Volume is an important measure because it is the best indicator of the relative size of one machine in comparison to another. Volume also indicates how bulky the unit is when car-

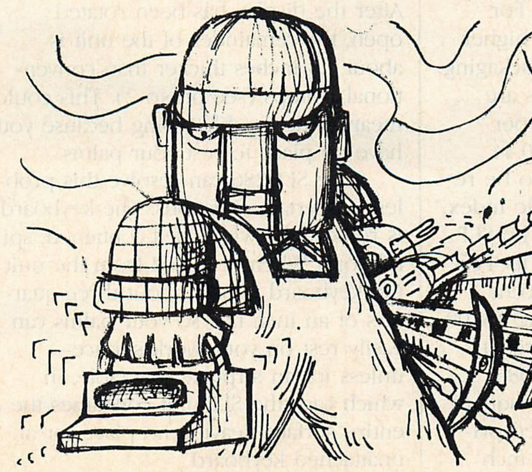

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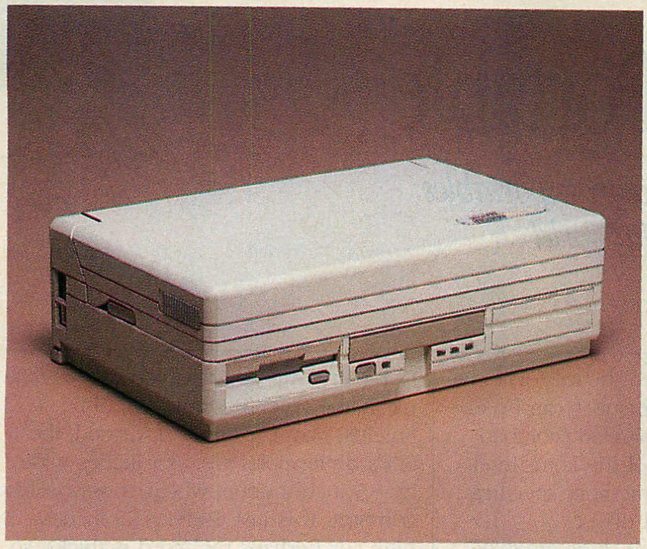
PHOTO 1: ***SLT/286—Ready to Travel***



Closed into its lunchbox profile, the SLT/286 is reasonably compact at 13.5 inches wide by 8.5 inches deep, yet at 4.25 inches high, it is thicker than most other portables.

PHOTO 2: ***SLT/286—Ready to Work***

Even with the display opened up, the unit remains on the thick side. The open position, however, reveals the laptop's readable, peppy, VGA-compatible LCD screen.

ried, an essential consideration in a portable. The SLT/286 has a volume of just over 476 cubic inches opposed to the T3100's 535 cubic inches; the SLT is, therefore, 11 percent smaller.

Weight is, of course, the most important measure when you are thinking about your shoulder. The carrying weight of the SLT is 14.2 pounds, including optional modem, compared with the T3100 at 14.7 pounds. The addition of the AC adapter to the SLT package raises its weight to almost 16 pounds. Most travelers will probably opt for the flexibility of using either the built-in battery or AC adapter, so 16 pounds is perhaps the more accurate figure. Keep in mind that the T3100 does not have a battery option.

A related measure, density, is the weight divided by the volume and yields an indication of how tightly the weight is packed into the unit. For machines of similar weights, a higher density thus reveals a tighter packaging. The densities of both machines are similar: the SLT is 0.48 ounces per cubic inch, and the T3100's is 0.44.

Footprint, which could also be referred to as the airline tray-table index, is width multiplied by depth. The SLT really has an advantage in that its 115-square-inch footprint is 32 percent smaller than the footprint of the T3100 (168 square inches) and 20 percent smaller than even that of the 8086-based Toshiba 1200 series (144 square inches). This advantage is gained primarily because of the SLT's 8.5-inch depth, which is 39 percent shallower than the T3100 and 29 percent shallower than that of the T1200. This advantage, however, is somewhat offset by the added thickness of the SLT.

Finally, lapload, measured in ounces per inch, indicates how heavy the unit feels sitting on your lap. Given two laptops of similar weight, the one with the smaller footprint will not spread the weight across as large an area, and thus will feel heavier. The lapload of the SLT is 1.98 ounces per square inch, 42 percent "heavier" than the T3100 at 1.40 ounces.

These measurements clearly put the SLT/286 in the same ballpark with other high-performance portables, with perhaps an edge accruing to Compaq because of the unit's shallow depth. A possible problem with the SLT involves the previously mentioned thickness. After the display has been rotated open, the remainder of the unit is about 1.5 inches thicker than conventional laptops (see photo 2). This could mean some trouble typing because you have no place to rest your palms.

The SLT/286 can resolve this problem in certain situations. The keyboard is removable, with a self-contained, spiral cord. When removed from the unit, the keyboard is only about three-quarters of an inch tall, so your palms can easily rest on your work surface—unless it's an airplane tray table, in which case the SLT unit consumes the entire surface, leaving no place for an unattached keyboard.

You should also be aware that the keyboard configuration closely matches that of the IBM PC Convertible, including the horrible doubling up of the cursor keys with Home, End, PgUp, and PgDn, activated by pressing the special Fn key. This arrangement is particularly troubling for WordPerfect users, who will find that key sequences formerly requiring only the right hand will now need synchronization with the left. I wish Compaq would ignore "standards" and simply improve the situation.

LOOKING GOOD, SEEING WELL

The most unremarkable feature of the SLT/286 is the new ten-inch-diagonal, compensated supertwist LCD. Lest you accuse me of contradicting my earlier statement about this display, which is truly a tour de force, let me describe my first outing with the machine.

I spent about an hour working with the SLT/286 under the thoughtful gaze of Compaq executives. About halfway through this session, the Texans asked me how I liked the display. My reply was a shrug, as I had not thought much about it to that point. By the end of the session, however, I realized that my silence was a testament to the quality of the new technology.

When sitting down to work at a portable computer, most of us have come to expect minimal display quality. Veteran portable toters often say, "I love having the machine with me, but I wish the display were readable." If we see an extraordinarily good display, we

may comment. If we see one that is substandard, we certainly complain. But, if we see a display that is more or less what we expect, we take it completely for granted.

This was precisely my experience. Sure, I knew I was staring at an LCD, which may have lowered my expectations. But, I was also looking at a display that I could read, and one that even had reasonably peppy performance. It did not immediately occur to me that I was also looking at a considerable technical accomplishment.

Compaq, working with an unnamed, outside vendor, has designed a brand-new display system for portables. It has approximately the same aspect ratio as a CRT display, so no squashed characters or distorted graphics are evident. It is lit from behind with two low-power, neon fluorescent tubes that run the width of the display area.

The light from this dual source is dispersed across the height of the display with a layer of translucent material. Even with such dispersal, the neon tubes have greater intensity along their axes, so the designers also included a shadowmask, which is nothing more than a layer of opaque material with tiny holes over its surface. The holes in the mask, however, are small near the light source and larger toward the top and bottom of the screen, a technique that further evens out the light. A matte surface reduces glare, and two controls adjust the display, one for contrast and one for the intensity of the backlight.

The effect is quite good. The viewing angle is very wide; the minor variations in head position that would cause me to lose the image on a PC Convertible's LCD do not affect the Compaq display noticeably.

As for performance, *PC Tech Journal*'s system-performance benchmarks (see "High-level Measurements," Kent Quirk, September 1988, p. 54) rate the SLT's 16-bit display subsystem as 42 percent faster than Compaq's own 8-bit EGA and only 13 percent slower than Compaq's 16-bit VGA subsystem running in a 16-MHz Deskpro 386S. These are more than respectable results for a battery-powered, laptop machine.

The combination of size, performance, and readability makes the SLT/286's display one of the best, if not *the* best, portable displays around.

HOUR POWER

The desire to take desktop power on the road is not without its price. The compromise usually exacted is either an AC tether, as in the Toshiba 3100, or a very short operational life on batteries, as is characteristic of the GridCase 1530 from Grid Systems (see Product Watch, David Claiborne, August 1988, p. 131). Therefore, the other noteworthy accomplishment of the SLT/286 is the engineering that has gone into its power system.

Any power-conservation system for a portable has three parts. The first is obviously in hardware and simply involves finding the components that consume the least power for the level of functionality desired. A good example is the hard-disk drive Compaq chose for the unit (which not surprisingly comes from Conner Peripherals, in which Compaq has a considerable investment). The hard drive consumes only 2 watts of power while operating, yet delivers an average access time of 29 ms. In fact, the *PC Tech Journal* system-performance benchmarks rate the disk subsystem about 8 percent *faster* than the 40MB hard disk in the Deskpro 286.

The second aspect of power conservation also involves hardware. In order to conserve power, the SLT includes circuitry to allow components of the system to be powered down under software control.

Powering *up* components is usually expensive in terms of power consumption; therefore, the third aspect of power conservation is the software strategy to be used to deliver smooth performance. This strategy needs to weigh the probability that a device will be accessed during the next interval of time against the power consumed by running the device continuously for that same time interval. For example, powering the device down for ten minutes and then restarting it might be more efficient in terms of power consumption than keeping it running for those same ten minutes.

The SLT/286 can turn just about any part of itself off, all under the control of a power-conservation utility program called PWRCON, which supports user-configurable parameters. With an appropriate strategy in place, Compaq suggests, three continuous hours of operation are possible on a full battery, including the regular use of hard-disk and diskette drives. Unofficially, Compaq executives and engineers feel that longer durations are likely under the right circumstances. The potential buyer should be aware that shorter durations are also possible for disk-intensive applications.

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Three hours is not a great endurance time for a battery, but consider another aspect. Compaq has engineered the battery for very fast recharge cycles. With the SLT connected to the AC adapter and turned off, the battery completely recharges in only one hour—a fantastic time. If the machine is being used, the battery charges in three hours.

Considering my own travel patterns, I could probably have the SLT/286 available for most of a transcontinental flight and perhaps even all of it if I could find an outlet during the connecting layover. The machine could certainly be fresh every morning. With such short recharge times and with the SLT/286 working diligently to conserve the battery's charge, Compaq's estimate of three hours should be satisfactory to most portable laptop users.

It is hard to tell if this new laptop, Compaq's first, will find an enthusiastic market. Considering its brilliant display, high level of performance, no-compromises design, and minimal flaws (just the keyboard, really), Compaq would seem to have another hit on its hands. And, if you agree, you will pay the price. At $5,399 for the basic Model 20 (with 20MB hard disk) and $5,999 for the Model 40 (40MB hard disk), the SLT/286 is not meant for everyone.

Those who can afford it will certainly not be sorry.

COMPAQ'S OTHER BABY

One of the points I made in my August 1988 column ("IBM and Compaq Strike Again," p. 31) was that the smaller cabinetry of the Deskpro 386S was likely to form the basis of the entire Compaq desktop line. Compaq has just introduced the second machine to appear in that form factor, the Deskpro 386/20e (see Tech Releases, this issue, p. 38).

The system needs little explanation once you know that Compaq has dropped the original Deskpro 386/20 from its line. In fact, it has also dropped the original 16-MHz 386 machine. Compaq now offers only the 386S at the 16-MHz performance level and the similarly configured 386/20e at 20 MHz (the Portable 386/20 is still available). The 386/25 remains in the original cabinet, offering the maximum expandability in the largest system unit.

A trend is probably lurking here. I suspect that Compaq will repackage its top-of-the-line computer whenever it announces a faster one. When the 33-MHz 386 machines arrive, therefore, the 25-MHz machine will earn its *e* designation and smaller form factor, while the faster machine will go in the old Darth Vader box.

The price of the 386/20e is $5,199 for a system with no hard disk, $6,599 for 40MB, and $7,999 for 110MB. By comparison, the 386/20 was priced at $7,499 with a 60MB hard disk, $9,499 for 300MB, and $12,499 for 300MB. As with the Deskpro 386S, the serial, parallel, and mouse ports are standard, as is a 1.2MB diskette drive and Compaq's VGA subsystem.

The VGA has been reduced to a chip instead of the piggyback board found in the 386S; expect the chip to show up in the 386S soon. Like the discontinued 386/20, the 386/20e includes the 82385 cache controller and a socket for either the Intel 80387 or Weitek 3167 coprocessor. Those wishing to have both coprocessors must now turn to the only Compaq machine so equipped, the 386/25.

The new machine and its new, lower price make the Compaq line more competitive with IBM's PS/2 Model 70. At $7,999, the 386/20e costs the same as the 20-MHz Model 70-121 *and* delivers 25 percent faster performance (the 70-121 does not use the cache controller), contains Compaq's fast, 16-bit VGA, and features a faster disk subsystem. The 386/20e also supports 5.25-inch and 3.5-inch diskettes and can have either a second hard disk or an integral tape backup unit. It also offers one more expansion slot than the PS/2 and does not need to use a slot for even the largest 16MB memory configuration. IBM's only remaining advantages are 10MB more disk capacity (worth about $136) and the Micro Channel (worth yet to be determined).

The PS/2 Model 70 just got a lot less attractive.

VGA NEWS

The 16-bit VGA revolution was kicked off by Paradise Systems Inc., which supplied its chip to Compaq for its VGA subsystem. Compaq's display performance took a significant leap ahead of the competition; more important, it called attention to the advantages of a 16-bit design. Other manufacturers followed suit with third-party boards, such as AST's VGA Plus.

The situation in the VGA market is similar to what happened in both the CGA and EGA markets, with some differences. One difference is that IBM builds the chip into every PS/2, so as

VGA technology advances, those machines will be candidates for upgrades. A more significant difference is that the VGA market is advancing quickly, with many products that extend the VGA specification to include higher-resolution modes or more colors.

Recent announcements from two chip manufacturers make the market even more interesting. Chips & Technologies (C&T) and Ahead Systems Inc. have designed VGA chips for specific market niches.

C&T has a chip designated as the 82C455, which is targeted for portable applications and is part of its LeAP (low-power enhanced AT portable) chip set. The chip supports either 8- or 16-bit data paths, can drive a variety of the emerging 640-by-480 flat panel displays, can handle up to 16 gray levels, and can map color to gray scales in a way that ensures legibility. The chip also supports EGA, CGA, monochrome, and Hercules modes and has power-conservation modes. C&T hopes to capture a share of the portable market with the LeAP chip set; we are likely to see some company following in Compaq's portable footsteps soon.

Ahead Systems' new chip is the AVGA. The two characteristics that make this chip so interesting are its higher performance and its extended modes. Ahead Systems claims that its proprietary design for the AVGA enables it to increase drawing speed 800 percent over other VGA solutions, which would make it the fastest game in town. The chip also directly supports more color and higher resolutions.

At 640-by-480 resolution, for example, the AVGA supports 256 colors out of more than 256,000, as opposed to IBM's 16. Furthermore, the AVGA offers 256 colors in an 800-by-600 resolution and 16 colors at 1,024-by-768, the latter being the same as IBM's optional 8514/A adapter. One higher resolution, 1,280-by-960, provides monochrome output. The AVGA chip thus offers not only much higher performance, but also 8514/A-like capabilities in the same amount of space in which IBM delivers basic VGA support.

Other contenders undoubtedly will pop up in this market. It is clear that, once again, IBM has lost control of its own standard, much to the benefit of the marketplace.

MACWORLD DISAPPOINTS

We all keep hearing how Macintosh is making such strong inroads into corporate America, propelled primarily by the strength of the huge and sophisticated base of graphics software for publishing and business-presentation graphics and the high level of interest in its ease of use. For the Mac to be successful in business, however, it must also support the software and hardware components necessary to allow its integration into the corporate environment. These components are already present for the PC. The Mac and PC universes actually complement one another—where the PC is strong, the Mac is weak, and vice versa.

During past visits to MacWorld, the computer industry's major Mac-only show, I saw evidence of growing attention to the real requirements of business. I also saw evidence of real interest in these developments by the attendees. This was true even as recently as last January in San Francisco. In Boston's MacWorld show in mid-August, however, I came away with quite a different opinion.

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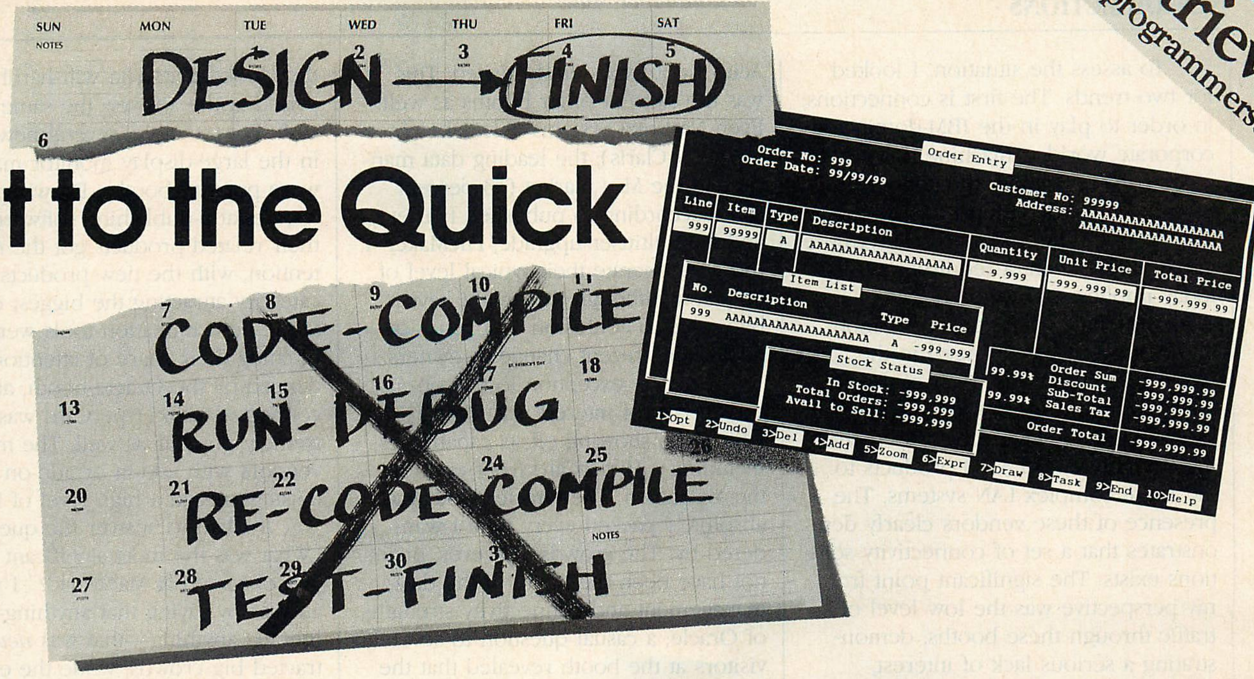

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To assess the situation, I looked for two trends. The first is connections; in order to play in the IBM-dominated corporate world, a machine first has to connect to it. Second, the connected machine must be able to handle the data residing on the hosts or anywhere else in the system, a requirement that today implies sophisticated data-management software at the desktop.

Not much has changed in the world of connections. Most of the known vendors of such products were present and showing their wares, from the straightforward 3270 products to the more complex LAN systems. The presence of these vendors clearly demonstrates that a set of connectivity solutions exists. The significant point from my perspective was the low level of traffic through these booths, demonstrating a serious lack of interest.

The light traffic in this area seemed to converge on the TOPS and Novell booths. That TOPS continues to generate interest is hardly surprising, and Novell has strengthened its offering with Mac support in recent releases of NetWare. By comparison with traffic at a Novell booth at Comdex or PC Expo, however, you could hardly call the level of interest high.

I paid a visit to the booth of every vendor of data-management software and was stunned by what I found—or, more to the point, what I did *not* find. In January, for example, Acius's booth showing 4th Dimension was packed—it was the hottest new data manager on the block back then. By August in Boston, enthusiasm had dimmed and the Acius booth was lightly visited. This was the story at other booths as well. Even Nashoba Systems' FileMaker (now made by Claris), the leading data manager in the Mac market (43 percent share according to published figures), and its multiuser upgrade, FileMaker 4, did not generate their typical level of attention, although that might have been due to confusion as a result of FileMaker's recent change in owners.

The one exception to this observed lack of interest was Oracle, which was showing off its capabilities, including a HyperCard front end for the Macintosh. The Oracle booth was absolutely packed every time I wandered by. The crowds, however, might not have been the result of the data-management and connectivity strengths of Oracle; a casual question to several visitors at the booth revealed that the HyperCard connection is what had drawn them in.

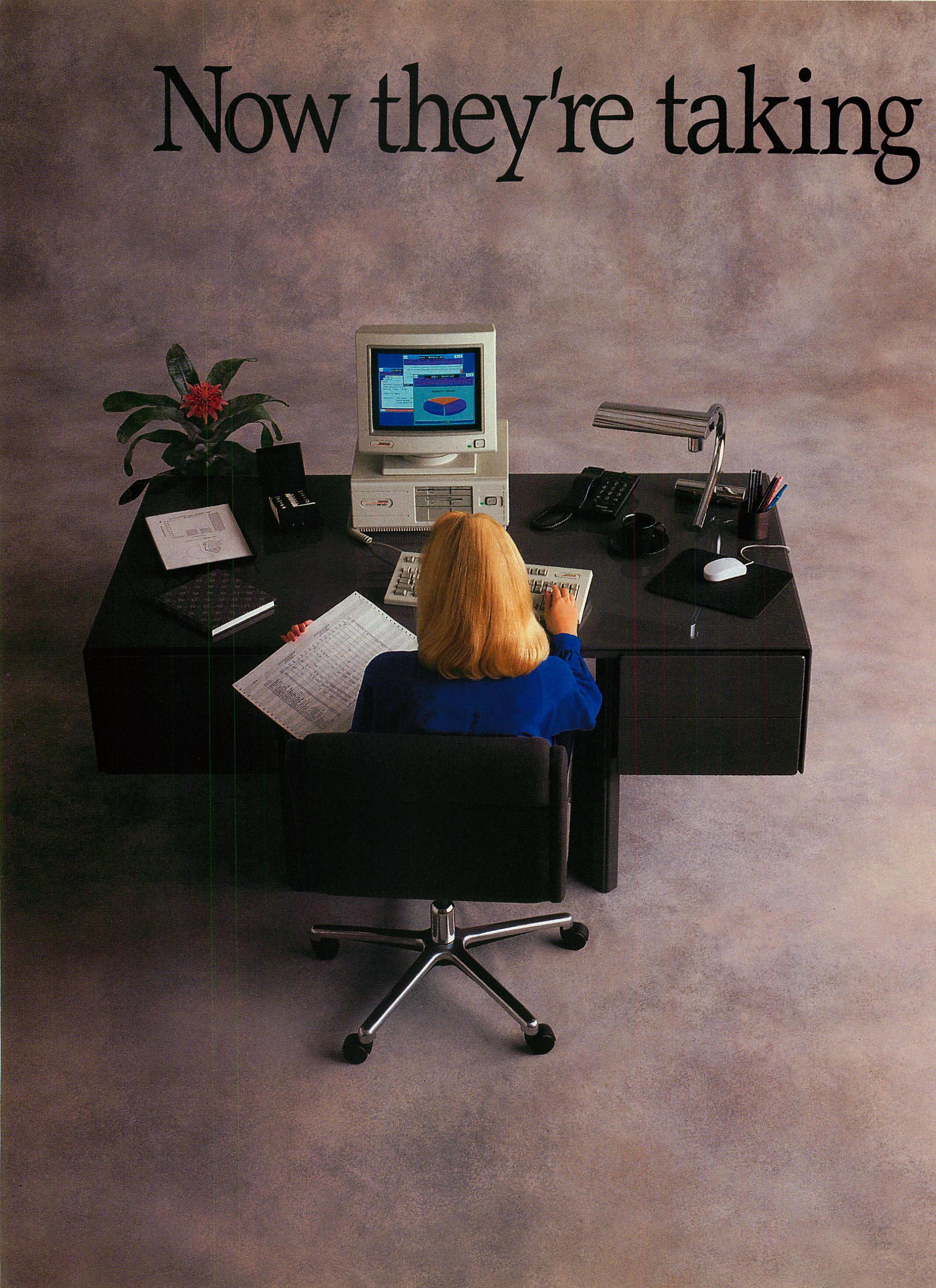
At a panel session entitled "Status Report: Mac Databases," attendance was light; the room was less than half full. I would have expected a bigger crowd if data management were a hot issue in the minds of the show's attendees. Furthermore, rather than providing an update on the state of the data-manager market, most of the panelists used the opportunity to advertise their companies' products. All of them spoke mostly from the standpoint of personal information needs (as opposed to corporate data management).

If the attendees at MacWorld were not interested in connecting with and processing corporate data, what *were* they looking at? You will hardly be surprised at the answer: the same old stuff. For example, several new entrants in the large-display monitor market were popular booths. Drawing, graphics, desktop-publishing software, and their related products got the most attention, with the new products in the category attracting the biggest crowds. Some new animation tools were also catching their share of attention. As evidenced by the Oracle booth, anything connected with HyperCard was extremely popular as well. The many new vendors with add-in or add-on hard disks garnered a high level of interest.

If I had to answer the question, "What was the most significant trend you observed at MacWorld?" I would answer by saying that anything—literally anything—that was *new* attracted big crowds, while the established products received less attention. This, in combination with my other observations, convinces me that Macintosh lives in an immature market, one not quite ready to do corporate business. It was the kind of show that would dazzle an art director, graphic artist, or newsletter publisher, but would probably turn off systems developers and integrators.

Why can't Mac get its corporate act together? Isn't this a burning issue at Apple? Whatever the answer to these questions, this is certain: if Mac doesn't learn to play better ball, it can forget about joining the big leagues.

Will Fastie is editorial director and founding editor of PC Tech Journal.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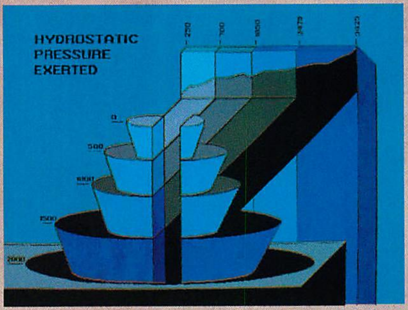

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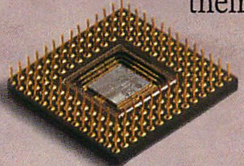
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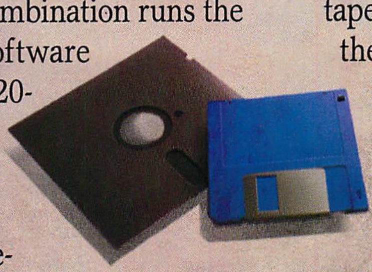
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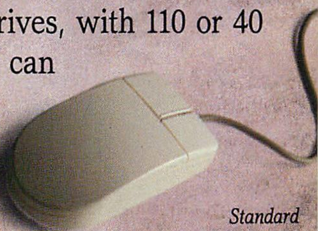
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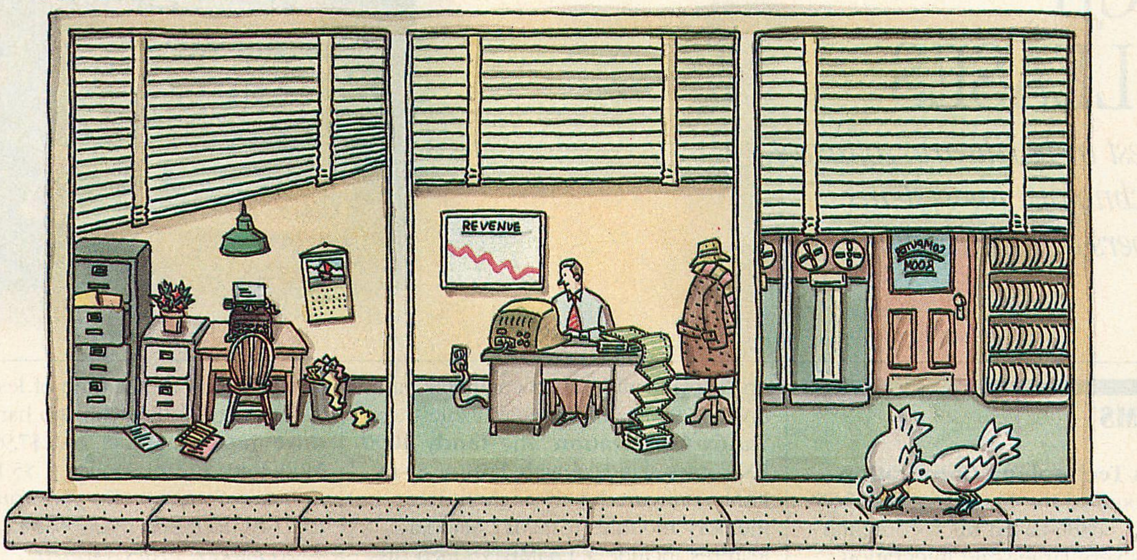

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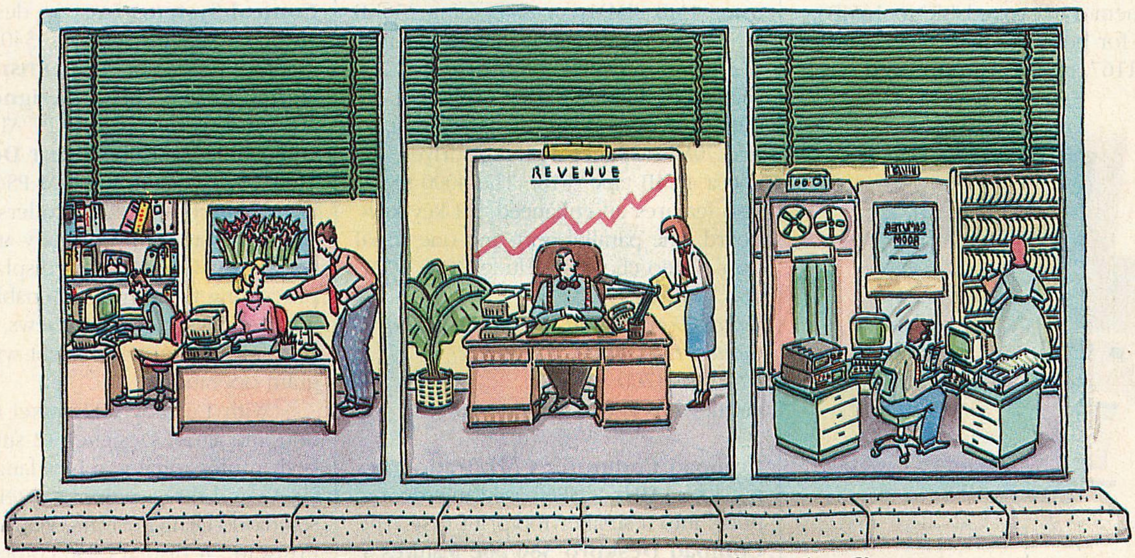

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Proteus-386/25GT 25-MHz microcomputer

Proteus Technology Corporation, 377 Route 17, Airport 17 Center, Hasbrouck Heights, NJ 07604; 800/782-8387; 201/288-8629

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An AT-compatible microcomputer based on the 20-MHz 80386 is available from **Tandy Corporation**. The **Tandy 4000 LX** comes standard with 2MB of 80-ns RAM, configured with single in-line memory modules (SIMMs). Standard features include a 1.44MB 3.5-inch diskette drive, support for an optional 20-MHz 80387, eight expansion slots (six 16-bit and two 8-bit), and a 32-bit memory-expansion slot. The optional memory-expansion board allows a maximum memory configuration of 16MB using 1MB SIMMs, or 8MB using 256KB SIMMs. Storage options include 3.5-inch (720KB or 1.44MB) and 5.25-inch (360KB or 1.2MB) diskette drives; 20MB (65-ms), 40MB (40- or 28-ms), and 70MB (28-ms) hard-disk drives; and a 40MB tape drive. The 4000 LX also features an enhanced 101-key keyboard, one parallel port, and one serial port. Video choices include CGA, EGA, and VGA. $3,999.

Tandy Corporation, 1700 One Tandy Center, Fort Worth, TX 76102; 817/390-3700

CIRCLE 302 ON READER SERVICE CARD

Compaq Computer Corporation has put its 20-MHz 80386-based microcomputer into a smaller footprint case. The **Compaq Deskpro 386/20e** features a cache controller with 32KB of 32-ns static RAM, built-in VGA capability, support for both a 20-MHz Intel 80387 or Weitek 3167, and serial, parallel, and pointing-device ports.

Model 110 comes standard with 1MB of 32-bit memory, one 1.2MB 5.25-inch diskette drive, one 110MB hard-disk drive with an access time of less than 25 ms, four expansion slots (8- or 16-bit), and one 32-bit memory-expansion slot (which can accept a maximum of 16MB). An optional 1.44MB 3.5-inch diskette drive is available. **Model 40** and **Model 1** have the same features as the Model 110, except that Model 40 has a 40MB hard-disk drive with an access time of less than 29 ms, and Model 1 has no hard-disk drive installed. Model 110, $7,999; Model 40, $6,599; Model 1, $5,199.

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CIRCLE 301 ON READER SERVICE CARD

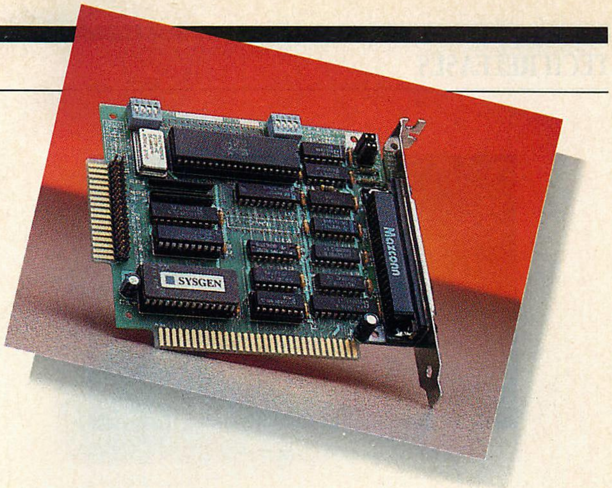
PERIPHERALS

Three graphics controllers offered by **Control Systems Inc.** are designed around Texas Instruments' 34010 graphics processor. The **ARTIST Designer 12** and **ARTIST Designer 16** are versions for the IBM PC/AT and compatibles, and the **ARTIST Designer 16MC** is a version for IBM PS/2 models. All three of the controllers use Control System's proprietary ARTIST GT software driver that uses display-list-processing techniques to enable no-wait redraws, bird's-eye views, and zooms and pans concurrent with program operation.

With 1,280-by-1,024 pixel resolution, the ARTIST Designer 12 supports both professional graphics language (PGL) and direct graphics interface standard (DGIS) drivers, via on-board firmware. It displays 256 colors from a 16.7-million color palette and operates at a 64-KHz horizontal scan rate at a 108-MHz bandwidth. It includes 512KB of on-board dynamic RAM; frame-buffer memory is handled by 1.25MB of on-board video RAM. $4,495.

The ARTIST Designer 16 and 16MC models both offer 1,664-by-1,200 pixel resolution for monochrome applications. They support DGIS drivers and deliver detailed, flicker-free, noninterlaced images. The Designer 16 offers software-selectable 1- or 2-bit-per-pixel operation, with a display window of 4,096-by-2,048 or 2,048-by-2,048 pixels. The Designer 16MC model offers 2-bit-per-pixel operation, with the same

The small-footprint Compaq 386/20e

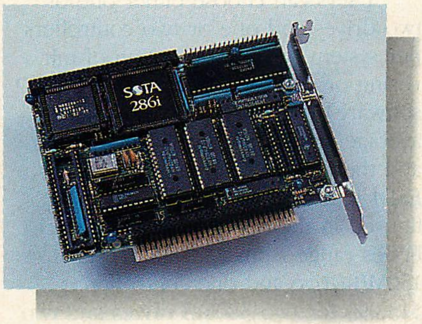


Omni-Bridge diskette-drive controller from Sysgen

functionality. It allows four shades of gray to be displayed at a resolution of about 150 dots per inch on a page-size monitor (comparable to the output of a 300-dot-per-inch laser printer). ARTIST Designer 16 and 16MC, $3,995 each. *Control Systems Inc., 2675 Patton Road, St. Paul, MN 55113; 800/826-4281; 612/631-7800*

CIRCLE 304 ON READER SERVICE CARD

An 80286-based accelerator board for 8088/86-based PCs is shipping from **SOTA Technology Inc.** The **SOTA 286i** half-size board comes with a 286 operating at 10 or 12.5 MHz, 16KB of high-speed RAM cache memory (expandable to 64KB), and support for an optional 80287. The SOTA 286i board also offers a 16-bit local bus connector for adding options that include the **Memory/16i**, which supports version



SOTA Technology's SOTA 286i accelerator board

4.0 of the Lotus/Intel/Microsoft expanded memory specification (EMS) or the extended EMS (EEMS) option that allows running OS/2. The board's toggle switch permits switching back and forth between 286 and 8086/88 modes. A connector is provided for the **Floppy I/O Plus**, a multimedia disk controller that supports as many as four diskette drives of varying densities, including high-density 1.2MB and 1.44MB diskette drives. It contains both a parallel port and serial port, with an optional second serial port. SOTA 286i-10 (10-MHz), $495; SOTA 286i-12 (12.5-MHz), $595; Memory/16i (with 0KB), $295; Floppy I/O Plus, $149. *SOTA Technology Inc., 657 N. Pastoria Avenue, Sunnyvale, CA 94086; 800/237-1713; 408/245-3366*

CIRCLE 307 ON READER SERVICE CARD

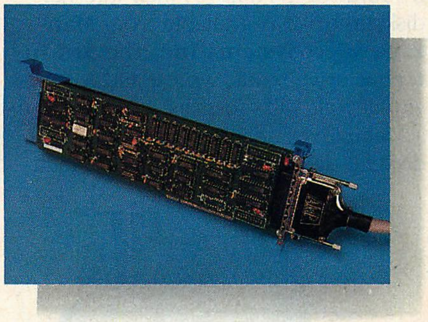
A coprocessor board for the Apple Macintosh II provides MS-DOS software compatibility and 1MB of expansion memory when not running DOS applications. The **MAC/DOS II** from **PerfecTEK Corporation** includes an IBM-compatible parallel printer port in addition to the printer port on the Mac II, as well as an IBM-compatible RS-232 communications port. Also included are disk-conversion and file-transfer utilities, and cable for direct transfer of files from PC to Macintosh computers. The MAC/DOS II is based on the Intel 80286 running at 5 MHz, and it supports an optional 80287. $1,495. *PerfecTEK Corporation, 1455 McCarthy Blvd., Milpitas, CA 95035; 408/263-7757*

CIRCLE 312 ON READER SERVICE CARD

A diskette-drive controller that provides access to all standard diskette drives for IBM PC, PC/XT, and PC/AT machines has been introduced by **Sysgen Inc.** The **Omni-Bridge** half-slot board supports 3.5-inch (720KB or 1.44MB) and 5.25-inch (360KB or 1.2MB) diskette drives as well as QIC-40 tape backup drives. Omni-Bridge controls as many as four diskette storage devices in any combination, and it can replace or coexist with the current diskette-drive controller. $95. *Sysgen Inc., 556 Gibraltar Drive, Milpitas, CA 95035; 800/821-2151; 408/263-4411*

CIRCLE 310 ON READER SERVICE CARD

A nine-track magnetic-tape controller board for IBM PS/2 Micro Channel computers is offered by **Overland Data Inc.** The **XL/2** has no switches or jumpers to permit easy installation, and it offers multiblock buffering on the board for increased performance of streaming-tape drives. DMA is not used, allowing more efficient data transfer. The XL/2 controller board works with any Pertec/Cipher-formatted nine-track tape transport, and it can interface with



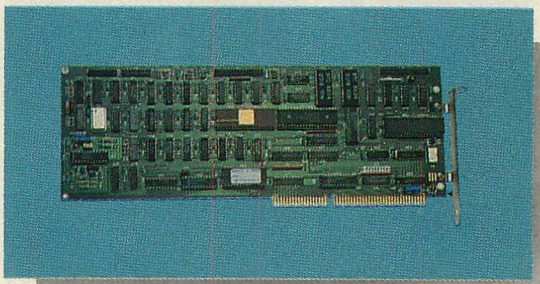
Overland Data's XL/2 tape controller board

most industry-standard formatted tape drives; it can read PE, NRZI, and GCR formats at 800, 1,600, 3,200, and 6,250 bytes per inch. The board controls tape drives with data-transfer rates faster than 900,000 bytes per second. $1,395; optional Xenix 386 driver, $995. *Overland Data Inc., 5620 Kearny Mesa Road, Suite A, San Diego, CA 92111; 619/571-5555*

CIRCLE 311 ON READER SERVICE CARD

A 2-8MB memory board for IBM PS/2 Models 50 and 60 has been unveiled by **Tall Tree Systems**. The **JRAM\2** fully implements version 4.0 of the Lotus/Intel/Microsoft expanded-memory specification (EMS) and extended EMS (EEMS) through hardware, and it runs in systems with processor speeds as high as 16 MHz. The memory board's modular piggyback design permits it to exceed 4MB using only one slot. User-installable RAM consists of 120-ns 1MB DIP RAM chips. JRAM\2 supports the full set of Micro Channel DOS registers and complete translation

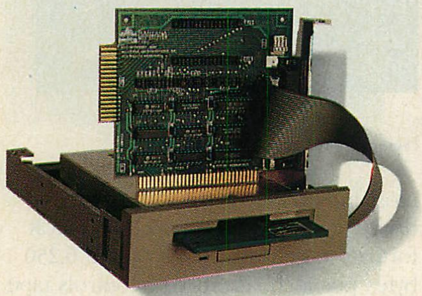
CORE LAN Subsystem from CORE International



Perstor PS180-16F diskette/hard-disk drive controller

RAM. The board features switchless installation and memory relocation, and it is completely software configurable. With 0KB, $399.
Tall Tree Systems, P.O. Box 50690, 2585 E. Bayshore Road, Palo Alto, CA 94303; 415/493-1980
CIRCLE 306 ON READER SERVICE CARD

A 720KB or 1.44MB 3.5-inch internal diskette drive is available from **Manzana MicroSystems Inc.** The **3rd Internal** drive reads, writes, and formats virtually all DOS formats. It comes with a Multiplexer Adapter Card, a 3.5-inch diskette drive mounted in a 5.25-inch



Manzana MicroSystem's 3rd Internal 3.5-inch diskette drive

frame, and internal cabling. The 3rd Internal also features Manzana's 3Five software, which includes a device driver and format program that gives users 720KB or 1.44MB of storage using any version of DOS from 2.0 to 3.3. 720KB, $299; 1.44MB, $340.
Manzana MicroSystems Inc., P.O. Box 2117, Goleta, CA 93118; 805/968-1387
CIRCLE 309 ON READER SERVICE CARD

Intel Corporation's Personal Computer Enhancement Operation (PCEO) has announced the release of **Above Board Plus** and **Above Board Plus I/O**, both of which feature support for version 4.0 of the Lotus/Intel/Microsoft expanded memory specification (EMS) and OS/2 hardware support for multitasking capability above 640KB. Above Board Plus can provide as much as 8MB of memory with an optional 6MB piggyback memory board. Above Board Plus I/O is identical to Above Board Plus, except that it comes standard with one serial and one parallel port. Above Board Plus, $795; Above Board Plus I/O, $945; 2MB piggyback board, $2,195.
Intel Corporation PCEO, Mail Stop C03-07, 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124-6497; 800/538-3373; 503/629-7354
CIRCLE 308 ON READER SERVICE CARD

Additions have been made by **Perstor Systems Inc.** to the **PERSTOR 200 Series** of 16-bit controllers that incorporate its proprietary Advanced Data Recording Technology. The **PS180-16F**, **PS200-16F**, and **PS180-16FHP** are diskette/hard-disk controllers for 80286- and 80386-based microcomputers, with processor speeds as high as 25 MHz.

The PS180-16F and PS200-16F models can increase hard-disk capacity by 90 and 100 percent, respectively, and they are port-address and register-set compatible with the IBM PC/AT controller. Features include a 16-bit bus, dual RAM, zero-wait-state data transfer, and an on-board BIOS supporting more than 60 types of hard-disk drives. Each controller manages two hard-disk drives and two diskette drives. Any combination of 3.5-inch (360KB or 1.2MB) and 5.25-inch (720KB or 1.44MB) diskette drives can be added to run concurrently with the hard-disk drives. The PS180-16F operates at 9 Mbps and allocates 32 sectors per track; the PS200-16F operates at 10 Mbps and allocates 34 sectors per track. PS180-16F, $345; PS200-16F, $365.

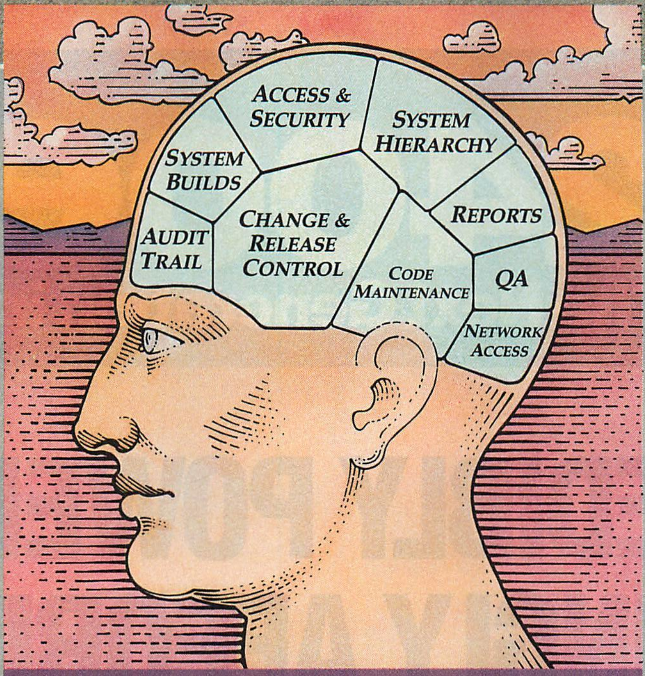
The PS180-16FHP offers the same features as the PS180-16F model, but it also includes a BIOS-resident cache that runs in any selectable combination of normal internal memory, the Lotus/Intel/Microsoft expanded memory specification (EMS), or AT extended memory. This disk-caching capability increases the system data-transfer rate to between 800KB and 4,000KB per second. $375.
Perstor Systems Inc., 7631 E. Greenway Road, Scottsdale, AZ 85260; 602/991-5451
CIRCLE 305 ON READER SERVICE CARD

CONNECTIONS

Mass-storage LAN subsystems designed for use with Novell NetWare, IBM Token-Ring, PC-NET, 3Com, and other major networks have been developed by **CORE International**. Ranging in capacity from 150MB to 760MB, the **CORE LAN Subsystems** are compatible with 80286- and 80386-based AT-bus machines.

Users can choose either one or two drives and one or two controllers per system (giving the option of mirroring or duplexing under Novell's SFT software). The LAN Subsystems have average access times of 16 ms or less, and they feature a high-performance ESDI interface. They come preconfigured in their own external cabinets. Prices range from $3,999 for one 150MB drive and one controller to $13,099 for two 380MB drives and two controllers (for duplexing).
CORE International, 7171 N. Federal Highway, Boca Raton, FL 33487; 407/997-6055
CIRCLE 319 ON READER SERVICE CARD

Digital Communications Associates Inc. (DCA) has introduced **DCA 3270 APA Graphics**, a software upgrade that allows users of DCA's IRMAX, IRMALAN, and IRMAremote products to run multiple-host graphics sessions. Features include on-line panning and zooming capabilities and a hot key that lets users switch among as many as five host graphics sessions. $495.



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Jonathan Richey
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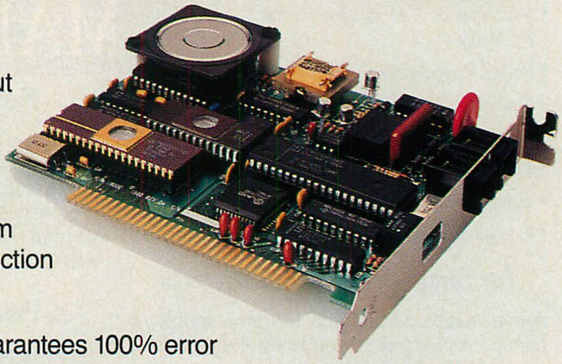
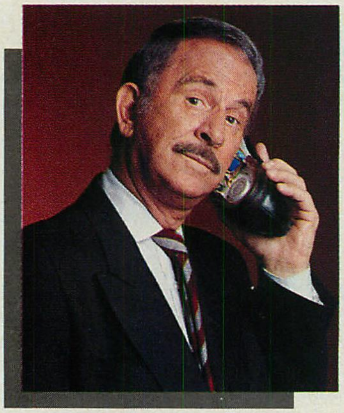


Imagine a modem so powerful it could deliver twice the throughput of a 2400bps modem. So reliable it would only send 100% error free data. Pick up a 2400etc and experience it.

The 2400etc is a high performance internal modem for the IBM PC/XT/AT and compatible systems. It includes an ATI custom designed digital signal processor which allows the modem to function on extremely noisy lines.



"Smart Idea"

The 2400etc with MNP level 5 guarantees 100% error free data transfer. And, using data compression, provides throughput speeds above 4800bps.

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The 2400etc operates in MNP and non-MNP modes and uses automatic feature recognition to establish a connection at the highest mutual error control level and operating speed.

Other standard features include 100% compatibility with the full standard and extended AT command sets. Adaptive dialing – Tone or Pulse, Automatic dial, redial and answer. Four communications ports 1, 2, 3, 4. Software controlled speaker etc, as ATI proudly calls it.

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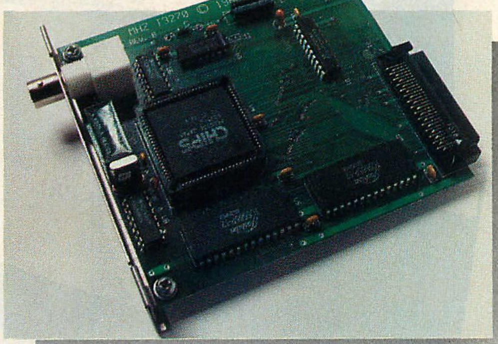
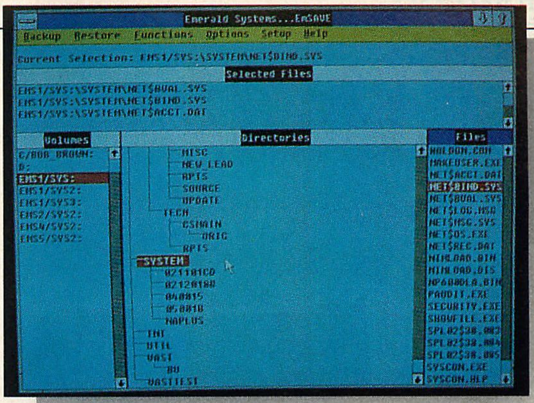


Megahertz Corporation's EasyTalk 3270 emulation board



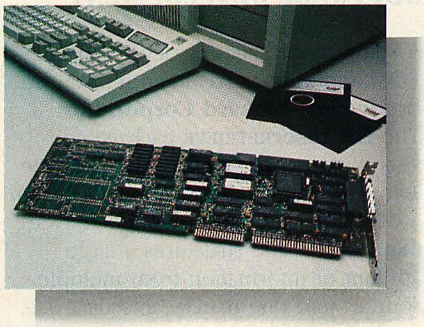
Emerald Systems EmSAVE screen with tree-format menu

DCA also announced **IRMALAN 802.2 Gateway**, which allows PC users on non-IBM or IBM NETBIOS-compatible LANs to access a 3270 mainframe computer through an IBM Token-Ring LAN. When the Gateway is used with a Token-Ring connection, as many as 64 PCs running IRMALAN SNA Workstation or APA Graphics software can access a 3270 mainframe. $595.

The company also offers **IRMAX DFT**, a software product for IBM 3278/79 terminal emulation that uses the enhanced connectivity capabilities of DFT technology to provide users access to a wide range of applications and functions. IRMAX DFT supports as many as five host sessions for 3278/79 terminal emulation. It also supports DCA's 3270 APA graphics-control program for access to mainframe graphics, and both DCA and IBM mainframe file-transfer software. Prices until January 31, 1989: bundled with hardware, $995; without hardware, $295 (thereafter, $1,195 and $395, respectively).
Digital Communications Associates Inc., 1000 Alderman Drive, Alpharetta, GA 30201-4199; 800/241-4762; 404/442-4000
CIRCLE 313 ON READER SERVICE CARD

A 3270 emulation board for Toshiba laptop computers has been announced by **Megahertz Corporation**. The **EasyTalk 3270** board fully supports all IRMA and IBM emulation, file transfer, and application software. It automatically configures itself to run IRMA or IBM software without the need for jumper changes. EasyTalk 3270 is packaged with IND$FILE support and 3270 emulation software. The board is compatible with IBM control units 3276, 3274, and 3174 in both CUT and DFT modes. $599.
Megahertz Corporation, 4505 S. Wasatch Blvd., Salt Lake City, UT 84124; 800/338-8726; 801/272-6000
CIRCLE 317 ON READER SERVICE CARD

Rabbit Software Corporation has produced **RabbitGATE II**, a family of LAN-gateway products that enables a user at a single DOS workstation on a LAN to connect to SNA, DFT, BSC, and X.25 mainframe sessions simultaneously from multiple windows, with concurrent DOS and notepad, via coaxial cable connections. All RabbitGATE II products are fully integrated, so a user needs to learn only one interface. The products offers optional all-points-addressable (APA) and S3G graphics support. **RabbitGATE II SNA**, 8-, 40-, and 64-session versions, $2,395, $5,995, and $7,995, respectively; **RabbitGATE II DFT**, $1,695; **RabbitGATE II BSC**, 8- and 32-session versions, $2,395 and $5,995, respectively; **RabbitGATE II X.25/PAD**, $2,495.
Rabbit Software Corporation, Seven Great Valley Parkway East, Malvern, PA 19355; 800/RABBIT-C; 215/647-0440
CIRCLE 318 ON READER SERVICE CARD

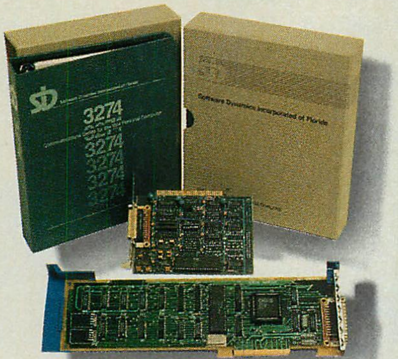


RabbitGATE II LAN gateway add-in board

A data-backup system for LAN administrators who perform backup-and-restore functions of multiple file servers has been introduced by **Emerald Systems Corporation**. The **EmSAVE** data-backup manager operates on the **RapidRecover** cartridge and cassette tape-backup subsystems. EmSAVE automatically locates available network-server files, disk volumes, and subdirectories and displays them in a tree-format menu for selection. In a restore operation, EmSAVE first presents the user with all save sessions currently found on the mounted tape, then graphically displays a tree of files and subdirectories available for backup. The RapidRecover subsystems series includes a 60MB cassette model (using .125-inch tape), a 60MB and 150MB cartridge model (using .5-inch tape), and a 300MB, dual-cartridge-drive subsystem (using .25-inch tape). EmSAVE applications kits include five data cartridges, a media storage case, software, and documentation. Cassette kit, $350; cartridge kits, $395 to $495; RapidRecover series, from $995.

Emerald Systems also offers **EmQ**, a data manager for use with Novell's Advanced NetWare. EmQ provides a shared backup-and-restore service for all users on a common PC network, regardless of network size. Users who access the server or bridge may execute backups from their local workstations or workgroup areas. When running under NetWare 2.1, EmQ accepts the files and directories specified by the user, checks the availability of the backup device, and then completes a backup. EmQ operates with Emerald System's VAST Device, a 2.2GB tape-backup subsystem with enhanced error-correcting code. The product includes the EmQ software, ten 2.2GB VAST cassettes, two user manuals, and a cassette storage cube. $1,495.
Emerald Systems Corporation, 4757 Morena Blvd., San Diego, CA 92117; 800/553-4030; 619/270-1994
CIRCLE 316 ON READER SERVICE CARD

Two products that combine the Microsoft OS/2 LAN manager and open systems interconnection (OSI) networking software have been released by **MICOM INTERLAN**, a division of **MICOM Systems Inc.** The **MICOM INTERLAN LAN Manager Unlimited** and the **MICOM INTERLAN LAN Manager Limited** allow users to


SDI3274 LAN Gateway for OS/2 from Software Dynamics of Florida

Freedom of Press from CAI

integrate the OS/2 LAN Manager standard into their OSI-based systems. The OSI networking software implements a Class 4 transport layer from data link through presentation, allowing end-to-end messaging reliability and flow control.

Other networking services supported include peripheral sharing, print spooling, and station-to-station messaging. LAN Manager Limited allows as many as five workstations to access a single server; the Unlimited version allows an unlimited number of workstations to do so. Both versions include OS/2 for the server. Unlimited, $2,195; Limited, $995.
MICOM Systems Inc., 155 Swanson Road, Boxborough, MA 01719; 800/526-8255; 800/835-5526; 508/263-9929
CIRCLE 314 ON READER SERVICE CARD

An enhanced LAN gateway for OS/2 has been developed by **Software Dynamics Inc. of Florida**. **Version 1.1** of its **SDI3274 LAN Gateway** emulates the functions of an IBM 3274 SNA/SDLC communications controller with attached terminals and printers. Host connections to IBM PC/ATs and compatibles or PS/2 machines can be accomplished via modem, DFT connection, or Token-Ring DLC. Terminal emulation software supports model 2, 3, 4, and 5 screen sizes; larger screens are viewed via scrolling and/or full-screen modes. Extended field and character attributes are available.

IBM-compatible (IND$FILE) file transfer can be used to move data between the PC and host, and IBM's high-level language application programming interface (HLLAPI) is supplied for users who want to write HLL programs to interface to the host via 3270 screen. Both SCS (LU1) and DSC (LU3) printer types are available; they are selected automatically for the user at SNA bind time. Print data can be routed to any PC printer or to a disk file. Price ranges from $750 for a 1-LU gateway to $3,210 for a 32-LU gateway.
Software Dynamics Inc. of Florida, P.O. Box 247, Dunedin, FL 34697-0247; 800/812-4734; 813/733-8784
CIRCLE 315 ON READER SERVICE CARD

SOFTWARE DEVELOPMENT

A software package for developing CD-ROM applications has been introduced by **Hewlett-Packard Corporation**. The **HP LaserRETRIEVE** package consists of two components: user-interface software that retrieves information from a CD-ROM, and database-build software that indexes and structures a large amount of information from multiple sources into one manageable database, ready for CD-ROM mastering. Once the CD-ROM is mastered and replicated, the HP LaserRETRIEVE graphics user interface allows the end user to search (with browsing and key words) and retrieve specified information from the CD-ROM. Single-license prices: user-interface software, $500; database-build software, $50,000.
Hewlett-Packard Corporation, Customer Information Center, 19310 Pruneridge Avenue, Cupertino, CA 95014; 800/752-0900
CIRCLE 320 ON READER SERVICE CARD

A product that allows printing of PostScript language files on ordinary printers is available from **Custom Applications Inc.** (CAI). **Freedom of Press** includes 35 fonts and an intelligent font-scaling system to allow infinite type sizes and rotation angles. Two versions are available: one uses Bitstream's Fontware and typefaces, and the other uses Compugraphics' Intellifont and typefaces. Freedom of Press allows supported 24-wire dot-matrix, ink jet, and laser printers to produce quality PostScript language output. It runs on the IBM PC/AT, PS/2 models, and 80386-based PCs and compatibles, using the machine's parallel port to send the page image in graphics mode to the supported printer. $495.
Custom Applications Inc., 5 Middlesex Technology Center, 900 Middlesex Turnpike, Billerica, MA 01821; 800/873-4367; 508/667-8585
CIRCLE 326 ON READER SERVICE CARD

Versions of **The Norton Utilities** and **The Norton Utilities Advanced Edition** that are compatible with DOS 4.0 are shipping from **Peter Norton Computing Inc.** Both utility packages now allow users to take advantage of the enhanced features of DOS 4.0, such as hard-disk drives larger that 32MB. The Norton Utilities, $100; The Norton Utilities Advanced Edition, $150.
Peter Norton Computing Inc., 100 Wilshire Blvd., 9th Floor, Santa Monica, CA 90401-1104; 213/319-2000
CIRCLE 325 ON READER SERVICE CARD

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Enhancements to **OPTASM 1.5**, an optimizing DOS assembler for 8086 and 80286 processors, have been added by **SLR Systems**. The product now provides programmers with on-line help (through the use of hot keys and overlapping help frames) and the ability to reference a particular command on the

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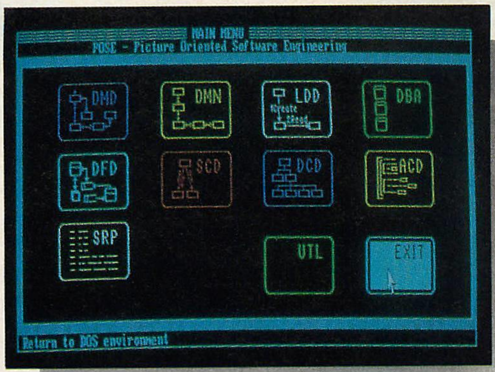
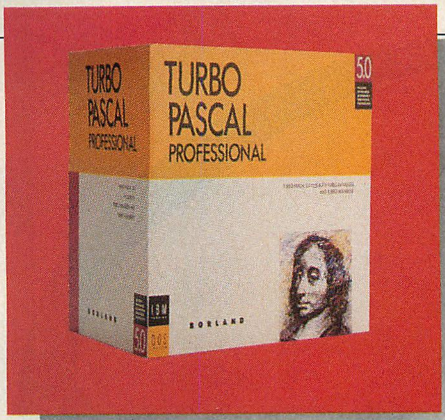


POSE screen from Computer Systems Advisers' CASE tool



Borland's Turbo Pascal Professional

screen while writing code using a special hyper key. OPTASM 1.5 also offers full support for Microsoft's CodeView debugger, full source debugging capability, and complete access to PUBLIC and LOCAL symbols. $125; upgrade, $29.95; demo disk, $10.
SLR Systems, 1622 N. Main Street, Butler, PA 16001; 800/833-3061; 412/282-0864
CIRCLE 329 ON READER SERVICE CARD

A computer-aided systems engineering (CASE) software development kit has been launched by **Computer Systems Advisers Inc.** The **POSE** (Picture-Oriented Software Engineering) kit comprises nine PC-based modules that address the planning, design, and analysis phases of application software development, using either data-driven or process-driven approaches. Each of the modules has a Macintosh-like user interface and facilities for data validation, integration, and normalization.

The Data Model Toolkit includes the Data Model Diagrammer, Data Model Normalizer, Logical Database Designer, and DataBase Aid; the Process Model Toolkit includes the Decomposition Diagrammer, Data Flow Diagrammer, Structure Chart Diagrammer, and Action Chart Diagrammer. The Screen and Report Prototyper is also available. Each module, $295; Data Model Toolkit (four modules) and Process Model Toolkit (four modules), $885; set of all nine modules (includes Screen and Report Prototyper), $1,770.
Computer Systems Advisers Inc., 50 Tice Blvd., Woodcliff Lake, NJ 07675; 800/537-4262; 201/391-6500
CIRCLE 321 ON READER SERVICE CARD

An enhanced realtime version of Unix for 80386-based microcomputers is being marketed jointly by **VenturCom Inc.** and **INTERACTIVE Systems Corporation**. **Version 3.1** of **Venix/386 System V** integrates INTERACTIVE Systems' 386/ix development environment and user interface with the realtime enhancements available in VenturCom's RTX/386 add-on module. The product's realtime capabilities include asynchronous I/O, preemptive priority scheduling, direct hardware access, virtual-memory allocation and in-core locking, and high-resolution alarms. Base system: two-user, $695; eight-user, $1,145. Including software development tools: two-user, $1,295; eight-user, $1,795.
VenturCom Inc., 215 First Street, Cambridge, MA 02142; 617/661-1230
CIRCLE 322 ON READER SERVICE CARD
INTERACTIVE Systems Corporation, 2401 Colorado Avenue, Santa Monica, CA 90404; 213/453-8649
CIRCLE 323 ON READER SERVICE CARD

An OS/2 version of **Teamwork**, a computer-aided systems engineering (CASE) product from **Cadre Technologies Inc.**, has been announced. Teamwork features include an intuitive graphics user interface; an open architecture

Cadre's Teamwork family of products running on a PS/2

and fully integrated environment; a central project database; an easy-to-use, context-sensitive graphics editing system; automatic project-information status tracking; version control of model generations; and implementation of structured methods, with consistency checking and understandable error reports. Single-user OS/2 version (bundled with Teamwork software analysis and design tools), $4,995; multiuser workstation-based version (to be available in early 1989), $7,500 to $15,900 for single-unit purchases.
Cadre Technologies Inc., 222 Richmond Street, Providence, RI 02903; 401/351-CASE
CIRCLE 330 ON READER SERVICE CARD

Enhanced versions of **Turbo Pascal** and **Turbo C** from **Borland International Inc.** offer built-in integrated and source-level debugging, new language extensions, and faster compile times. **Version 5.0** of Turbo Pascal provides dynamic overlay support, support for the Lotus/Intel/Microsoft expanded memory specification (EMS) for programs of any size, and 8087 floating-point emulations. **Version 2.0** of Turbo C features an optimizing C compiler, a MAKE facility with automatic dependency checking, and support for all six memory models. $149.95 each.

Borland also announced the **Turbo Assembler** and **Turbo Debugger**. The Turbo Assembler runs as much as three times faster than MASM, supports Turbo C in-line assembly and MASM, and is compatible with all 80*x*86 instruction sets. The stand-alone Turbo Debugger offers source and data-level debugging, overlapping windows, session logging, and support for a dual-monitor and EMS. $149.95.

The **Turbo Pascal Professional** and **Turbo C Professional** packages bundle the Turbo Assembler and Turbo Debugger with Turbo Pascal 5.0 and Turbo C 2.0, respectively. $250 each.
Borland International Inc., 4585 Scotts Valley Drive, Scotts Valley, CA 95066; 408/438-8400
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The material that appears in Tech Releases is based on vendor-supplied information. These products have not been reviewed by the PC Tech Journal *editorial staff.*

The VGA Compatibility Test

The proliferation of VGA adapters is as overwhelming as the number of colors on the VGA palette. Our new compatibility test suite helps you choose one that best meets your needs.

ED McNIERNEY and KENT QUIRK

The recent deluge of Video Graphics Array (VGA) adapters for PCs and compatibles is both a technicolor dream come true and a nightmare for users and systems integrators. The good news is you can benefit from the improved graphics performance of the VGA without having to buy an IBM PS/2 Model 50 or above—and you can negotiate on price and features.

The bad news is that the sheer number of adapters on the market—there are dozens, including ones from IBM, Compaq, Video Seven, and Paradise Systems—leaves room for error. Compatibility with the IBM standard is very important and difficult to judge.

To address this problem, *PC Tech Journal* has developed a VGA evaluation suite. Using the tests in the suite, *PC Tech Journal* in this article reviews IBM's PS/2 Display Adapter (for the PC, AT, and PS/2 Model 30) and Compaq's Video Graphics Controller (VGC). These two add-in adapters are reviewed initially because they are the first two major VGA-compatible boards to hit the streets. Other adapters will be reviewed in future issues. The compatibility tests are available on PCTECH-line (301/740-8383) so that readers can download and run them.

IBM's VGA is an improvement over the performance and functionality of the Enhanced Graphics Adapter (EGA). It is incorporated into the system boards of all PS/2 machines except the Models 25 and 30 (see "VGA: Evolutionary Half-Step," John T. Cockerham, August 1987, p. 74). It can display on screen up to 256 colors at a time from a palette of more than 256,000 using 320-by-200-pixel double-scanned mode or 16 colors from the same palette in 640-by-480 mode.

According to responses to a recent informal reader poll (see "Professional Viewpoint," Jordene Zeimetz, July 1988, p. 160), most *PC Tech Journal* readers already are enamored of VGA and are no doubt anxious to have this capability on their machines. When asked to grade IBM's PS/2 family of computers and its major components, most readers gave a thumbs-up to the VGA and 3.5-inch diskettes, while the Micro Channel architecture and the PS/2 family in general received a thumbs-down.

In your rush to acquire the VGA, however, it would be wise to resist the temptation to run out and buy the first or least-expensive board you can get. That board might not provide a high enough degree of compatibility with IBM's VGA, which is the standard most developers will use for writing their software. From a practical and economic viewpoint, these developers are more likely to test their software on IBM's system-board VGA than on the many third-party adapters. If an application does not run on a third-party adapter, fingers will point at the user and the board rather than the developer and the software.

Prices for third-party add-in adapters range from $350 to $600. Although all claim to provide compatibility with the IBM standard, some offer more compatibility and greater enhancements than others (which accounts for much of the price difference). Enhancements can include higher resolution and performance. Cost and enhancements are a consideration when deciding on any adapter, but for most people compatibility is the most crucial factor.

ILLUSTRATION • ANDY LEVINE

TABLE 1: ***BIOS Video Modes***

MODE	TYPE	SCHEME	COLORS[a]	RESOLUTION	GLYPH CELL
0H	Text	40-by-25	16	360-by-400	9-by-16
1H	Text	40-by-25	16	360-by-400	9-by-16
2H	Text	80-by-25	16	720-by-400	9-by-16
3H	Text	80-by-25	16	720-by-400	9-by-16
4H	Graphics	Split	4	320-by-200	8-by-8
5H	Graphics	Split	4	320-by-200	8-by-8
6H	Graphics	Split	2	640-by-200	8-by-8
7H	Text	80-by-25	Mono	720-by-400	9-by-16
DH	Graphics	Linear	16	320-by-200	8-by-8
EH	Graphics	Linear	16	640-by-200	8-by-8
FH	Graphics	Linear	Mono	640-by-350	8-by-16
10H	Graphics	Linear	16	640-by-350	8-by-16
11H	Graphics	Linear	2	640-by-480	8-by-16
12H	Graphics	Linear	16	640-by-480	8-by-16
13H	Graphics	Linear	256	320-by-200	8-by-8

[a] *Maximum number of colors that can be displayed simultaneously from a palette of more than 256,000 colors, except in monochrome mode.*

The VGA provides video modes supported on previous IBM adapters plus modes with 640-by-480 pixels in 2 and 16 colors, and 320-by-200 pixels in 256 colors.

This becomes more apparent as new software manipulates every feature and twist of VGA design and as VGA-compatible hardware manufacturers fail to reproduce the IBM VGA's functionality. There is no guarantee that they accurately emulate a set of hardware as complex as the VGA to the level required by the users of graphics applications. Even a small variation in the board's operation can be devastating if the feature that varies is essential to your application's operation.

How can you be sure the adapter you buy will pass muster? *PC Tech Journal*'s VGA evaluation suite uses a battery of compatibility tests to exercise documented features of the VGA. The goal is to discover variations or inconsistencies in individual VGA-compatible adapters and to provide real answers to users and systems integrators about how valuable, reliable, and compatible a given display adapter will be with application software. Undocumented features are not put through the grist mill because most software developers avoid using them.

COMPATIBILITY MEANS . . .

VGA compatibility seems to mean whatever the manufacturer of a VGA-compatible display adapter wants it to mean—each product's advertisements stress the value of its own type of compatibility, from a simple BIOS video-mode setting to support of the same applications as IBM but with a customized set of drivers to offset deficiencies or variations in the hardware. The two basic types of compatibility are at the BIOS level and the register level.

BIOS compatibility is the less stringent and less useful type. A BIOS-compatible display adapter adheres to the software programming interface provided by the IBM video BIOS specification. IBM originally provided this interface in the PC as a standard-access mechanism for a variety of different video-display hardware—at first, only for the Monochrome Display Adapter (MDA) and the Color Graphics Adapter (CGA). IBM has updated and expanded the interface to support video features available in subsequent machines.

Although the interface has been greatly enhanced and expanded with each new graphics adapter introduced by IBM, it is not powerful enough for high-performance text and graphics applications because it does not provide all available hardware functions. Those it does provide are much slower than the functions provided when the application accesses the hardware directly. These applications tend to use the BIOS function calls for inquiry operations and functions that are not performance critical. Almost every software product, however, bypasses the BIOS at one or more points to provide better display speed or functionality not supported by the BIOS but available on the display hardware.

For most users, BIOS compatibility is a necessary but insufficient level of performance in a VGA-compatible display adapter. Because it is easier to obtain than register compatibility, it has been featured in many early VGA-compatible products. As the market becomes increasingly sophisticated, such a level of compatibility will just not be enough for most users.

Register compatibility involves complete hardware emulation of the VGA's functionality. Most VGA functions and features are controlled by reading or writing to one or more of a large number of control registers on the display adapter. For compatibility, however, this term refers to complete hardware emulation of all I/O, memory, and interrupt features on the adapter—not just to the adapter's register set.

This kind of compatibility is like a Turing test for display adapters: a display adapter is considered register compatible with a PS/2 system-board VGA if an application program cannot distinguish between it and the real VGA. Such an application program is not restricted to BIOS function calls but is allowed to program the hardware in any manner it wishes in order to discover a difference in behavior between the two adapters.

The *PC Tech Journal* evaluation suite tests hardware and BIOS compatibility features as documented by IBM in order to provide the answer to the question: If I purchase or recommend this VGA-compatible display adapter, can I be confident that it will run the applications software I buy for it?

A ROBUST TEST

The tests in the evaluation suite measure BIOS function compatibility, BIOS data-area compatibility, alphanumeric support, register operation, and split-screen and scrolling operations. They test all meaningful combinations of register contents. The suite is designed to be a robust and vigorous test of a VGA's operation. It will tell developers and integrators if VGA-specific software can be expected to run properly on a given display adapter.

Speed benchmarks are not included in this evaluation suite. Performance of a particular adapter/computer combination can be tested using *PC Tech Journal*'s systems benchmarks presented in "High-level Measurements," Kent Quirk, September 1988, p. 54. The ultimate way to get accurate performance information is to test run applications on the display adapter combined with the system of interest.

The VGA evaluation suite requires minimal user interaction. Although some features are impossible to judge

without querying the user, every reasonable attempt has been made to determine the results of a test without requiring user input. For example, the BIOS mode test checks whether the adapter supports all the video modes required. This test attempts to set each mode through the BIOS, inquire from the BIOS about the characteristics of that mode, and then check the current video mode to determine whether it is the one just set.

Because one feature of the VGA is its powerful palette and color control, some of the tests require fairly subtle color discrimination. Anyone who cannot discern subtle color differences either can get a colleague to help out or should run the tests on a system that is equipped with a monochrome monitor. The tests that affect palette output will determine if a color or monochrome monitor is installed. If they detect the latter, the tests will scale down automatically to examine only the 64 levels of gray scale supported on a monochrome display.

THE BIOS PREREQUISITE

The suite tests all 23 major BIOS functions and the 15 video modes and 47 subfunctions that they include. Although the successful completion of these BIOS-evaluation tests should not be considered adequate for evaluating VGA performance, it is a prerequisite to full VGA compatibility.

In addition to standard BIOS functionality, the suite tests the state of all the VGA's readable registers after each function call and compares them with that of the register set of the IBM VGA. Some applications use BIOS calls to perform initialization operations such as mode setting and then directly to modify registers not set appropriately for the application's needs by the BIOS. Therefore, it is essential that the BIOS function calls of a compatible VGA not only perform the same overall operation but do so by programming the VGA register set in exactly the same manner as the IBM VGA. Each of the BIOS tests is described below.

Mode support. The VGA BIOS supports video modes 0 through 7 and 0DH through 13H (see table 1). The mode-support test uses BIOS function 0 (select video mode) to set each of the 15 video modes in turn. Then each mode is tested by using BIOS function 0FH (get video status) to check the number of text columns expected in that mode and to see that the mode selected is in fact the one reported by the BIOS. Text is displayed in each mode using BIOS function 13H (display character string) to help confirm the correct operation of each mode.

Cursor operation. The video BIOS provides several functions for cursor operation—both moving the text cursor and specifying its size. The test for this operation positions the cursor in various screen locations using BIOS function 2 (set cursor location) and selects various cursor sizes using BIOS function 1 (set cursor size). The results of these tests are confirmed by using BIOS function 3 (get cursor state) to check that the reported state is the same as that which was set. In addition, the user is asked to confirm that cursor-hiding attempts successfully remove the cursor from the screen.

Lack of light-pen support. Unlike the EGA, the VGA interface does not have light-pen support. BIOS function 4 (return light-pen position) is used to check that the VGA correctly reports that no light pen is installed. This check is necessary to assure the correct operation of applications that use a light pen if present.

For most users, BIOS compatibility is a necessary but insufficient level of performance in a VGA-compatible display adapter.

Multiple-page support. The BIOS can write text and graphics to multiple video memory pages when the adapter has sufficient memory for multiple-page support. To test this capability, BIOS function 5 (select active video page) displays each of many pages in several different video modes; BIOS function 13H (display character string) places text on each of the nondisplayed video pages before those pages are brought to the screen.

Screen scrolling. BIOS functions 6 (scroll up) and 7 (scroll down) allow rectangular regions of text to be moved on the display and to be erased completely. The screen-scrolling test uses BIOS function 13H (display character string) and function 8 (read character/attribute) to put text on the screen and read it back after it has been scrolled.

Text I/O. This test covers BIOS functions 8 (read character/attribute), 9 (write character/attribute), 0AH (write character at cursor), 0EH (write TTY), and 13H (display character string) to examine all BIOS text I/O. The text I/O test is performed in several video modes using function 0 (select video mode) to choose among modes.

Overscan control. The display adapter's overscan color for 16-color, 4-color, and 2-color text and graphics modes can be selected through the overscan-control function (0BH). This function also selects between the two 4-color palettes available in 4-color graphics modes. This feature is exercised in the palette-loading test.

Graphics I/O. To check graphics I/O for all graphics modes supported by the VGA, one of the compatibility tests in the evaluation suite evaluates BIOS functions 0CH (write pixel) and 0DH (read pixel). Every pixel on the screen is drawn and every possible pixel value available in the current video mode is used; then each pixel is read back to ensure that the correct value was written. For all but the 256-color graphics mode, pixels written can either replace the display-buffer data or be exclusive-or merged with it. The suite tests both modes of writing to the screen.

Mode inquiry. The mode-inquiry function 0FH (get video status) provides the current video mode, active video page, and number of text columns on the display. The test for this function validates the values returned by the function, including that of the active video page when multiple pages of display memory are in use.

Palette-register control. BIOS function 10H, set palette registers, contains 16 subfunctions to support a wide variety of palette-register control operations. Individual palette registers, digital-to-analog converter (DAC) registers, video-DAC-mask registers, and the display's overscan color can be programmed or read either individually or in blocks. All 16 subfunctions are tested and their performance is verified by this block of tests.

Character-generator support. BIOS function 11H, character-generator support, also incorporates a large set of subfunctions—22 of them. These operations all control the VGA's ROM and RAM-loadable character sets. Any of the three character sets stored in the VGA's ROM (8-by-8, 8-by-14, and 8-by-16 pixels) can be selected as the active character font for the display, or a user-defined character set can be loaded from system memory.

In addition to font selection, function 11H's subfunctions have a set of inquiry operations that provide infor-

mation about the VGA ROM character-set addresses and auxiliary-interrupt vectors used. The evaluation suite tests all ROM character sets for proper selection, sizing, and display.

Video configuration. BIOS function 12H, alternate select, supports nine subfunctions that return various bits of information about the current video-system configuration. A number of the video system's operations parameters can be selected through this function, including display switching, video-refresh control, CPU access to display memory, and gray-scale summing (used for mapping color to monochrome screens). The video-configuration test exercises BIOS functions 1AH and 1BH. Function 1AH provides inquiry and selection between a primary and a secondary video display; function 1BH fills out a 64-byte buffer with a complete set of functionality and configuration information about display adapter hardware and current mode settings.

All video-configuration information subfunctions except 35H are tested. This subfunction allows for switching between a PS/2 display adapter such as the IBM 8514/A and the PS/2 system-board VGA. Because VGA-compatible display boards are not designed to run on the PS/2, this function is not expected to perform any useful function on VGA-compatible boards.

Video-state save/restore. This BIOS function (1CH), added to help support multitasking operating systems, allows the complete control and hardware state of the VGA to be either read or programmed in a single operation. By combining this function with a read and restore of video-display memory, a complete screen state switch can be accomplished. The video-state save/restore test creates several different video-display and drawing states and switches among them, saving and restoring each one in turn.

TESTING DATA AREAS

The video BIOS is more than an interface to program the VGA's register hardware. It also maintains a complete set of data areas that contain important video-state and functionality information. Because these data areas are supported and documented, many applications use them to read video information directly rather than going through the BIOS. The following tests check that a display adapter properly maintains the information in this data area.

Standard data area. This block of information is stored at a fixed location in the video system's low memory. In seg-

TABLE 2: ***VGA Registers***

REGISTER TYPE	DESCRIPTION
GENERAL REGISTERS	
Miscellaneous output	Controls I/O address selection (to emulate either CGA or MDA), memory access control, pixel clock selection (for either 640 or 720 horizontal pixels), video synchronization control, memory addressing, and synchronization-signal polarity
Feature control	Supported for EGA compatibility; the values of its two low-order bits are driven to two output pins on the EGA's feature connector; also allows selection of an alternate vertical synchronization signal
Input status zero	Contains flag bits that allow identification of which VGA-compatible monitor is attached to the adapter, and whether a vertical retrace interrupt is enabled
Input status one	Holds a flag bit testing for the presence of any retrace period and another bit indicates whether or not a vertical retrace is in progress. A two-bit diagnostic field allows for testing all video output signals when used in conjunction with the color plane enable register
DAC INTERFACE REGISTERS	
DAC pixel mask	Selectively masks display buffer data before they are used as a DAC index value
DAC write data address	Selects address at which DAC data are written
DAC read data address	Selects address from which DAC data are read
DAC status	Shows whether last DAC operation was read or write
DAC data	Register to which DAC data are written or from which they are read
SEQUENCER REGISTERS	
Sequencer address	Selects which of the sequencer registers can be written to or read from the sequencer data register
Sequencer reset	Controls one of two levels of sequencer-reset operations
Clocking mode	Controls character-cell width, size of memory accesses, dot-clock division, and video refresh memory accesses
Map mask	Enables or inhibits CPU access to each of the VGA's four 64KB memory maps
Character map select	Selects which two of a maximum of eight loaded character sets are currently used in alpha modes
Memory mode	Reports amount of installed RAM, mapping of memory addresses to the four memory maps, and operation of sequential addressing of video memory
CRT CONTROLLER (CRTC) REGISTERS	
CRTC address	Selects which of the CRTC registers can be read from or written to at the CRTC data register
Horizontal total	Sets total number of pixels on each scan line
Horizontal display end	Sets address of last displayed pixel on each scan line
Start horizontal blank	Sets beginning of horizontal blank period
End horizontal blank	Sets end of horizontal blank period
Start horizontal retrace	Sets point at which electron scan beam starts moving back from the end of the scan line
End horizontal retrace	Sets point at which electron scan beam begins moving forward at the start of a new scan line
Vertical total	Sets total number of scan lines per video frame
Overflow	Holds high-order bits of some CRTC registers
Preset row scan	Controls fine vertical image scrolling
Maximum scan line	Sets the number of scan lines per character cell on the display and controls scan doubling to allow 400-line display of CGA 200-line video modes
Cursor start	Sets the scan line on which the cursor starts within the character cell
Cursor end	Sets the scan line on which the cursor ends within the character cell

REGISTER TYPE	DESCRIPTION
CRTC REGISTERS (Cont.)	
Start address high	High-order eight bits of the display buffer offset from which video data are displayed
Start address low	Low-order eight bits of the display buffer offset from which video data are displayed
Cursor location high	High-order eight bits of the character offset on which the cursor lies
Cursor location low	Low-order eight bits of the character offset on which the cursor lies
Vertical retrace start	Sets the scan-line address at which the scan beam begins to return to the top of the display
Vertical retrace end	Sets the scan-line address at which the scan beam begins moving down the display; controls vertical retrace interrupts, video memory refresh, and CRTC register write protection
Vertical display end	Sets address of last displayable line on the display
Offset	Sets the logical width of the display in character cells
Underline location	Sets scan line in each character cell on which the underline is positioned
Start vertical blank	Sets the scan line at which display blanking begins
End vertical blank	Sets the scan line at which display blanking ends and active video data begin
CRTC mode control	Flag bits controlling 6845 emulation, output control, horizontal retrace resolution, retrace enable, and character fetch address update
Line compare	Sets scan line at which the scan-line counter is reset to protect a part of the display from vertical scrolling
GRAPHICS CONTROLLER REGISTERS	
Graphics controller address	Selects which graphics controller register is read from or written to at graphics controller data register
Set/reset	Defines data written to each bit plane when set/reset is enabled or write mode 3 is used
Enable set/reset	Selects set/reset mode for each bit plane independently in write mode 0
Color compare	Defines color compare value used in read mode 1
Data rotate	Sets number of bits by which display data are right-rotated before being written in write modes 0 and 3
Read map select	Selects among four memory maps for CPU reads from display memory
Mode	Selects among four write modes, two read modes, and two video shift register load modes
Miscellaneous	Holds flags for graphics or alpha mode, memory-map-access modes, and VGA memory-address mapping
Color don't care	Selects bit planes in read mode 1 color comparisons
Bit mask	Selectively controls which pixels are modified during a byte-wide write
ATTRIBUTE CONTROLLER REGISTERS	
Attribute controller address	Selects which attribute controller register is read from or written to at attribute controller data register
Palettes (0–15)	Provides EGA-style selection of 16 physical colors from the current palette
Mode control	Provides attribute selection, eight- or nine-pixel character display, blink/intensity selection, panning control, palette selection, and data-output clock rate
Overscan color	Selects color value used for display's overscan
Color plane enable	Selectively allows or clears output from each of the four color maps
Horizontal pel panning	Allows the display image to be shifted left by a maximum of eight pixels
Color select	Selects high-order pixel value bits for all video modes with fewer than eight bits per pixel

The VGA is controlled using its general registers and DAC interface registers, along with registers in the sequencer, CRT, graphics, and attribute controllers.

ment 40H, offsets 49H through 0ABH hold a set of system parameters and pointers to additional data areas. The test of the standard data area exercises several VGA BIOS functions and checks that the data area is updated properly after each test is completed.

Primary-state save area. This auxiliary data buffer is used by both the EGA and the VGA. A double-word pointer in the standard data area points to it, and it contains a table of address pointers to parameter- and character-set definition tables. The test of the primary-state save area checks the contents of this buffer across several BIOS operations.

Secondary-state save area. Unique to the VGA, this area is pointed to by a double-word pointer in the primary-state save area. This buffer holds pointers to additional information new in the VGA, including user-palette tables and display combination tables.

Video-parameter table. This table holds the hardware CRT controller (CRTC) and other register values used in programming each of the video modes supported on the VGA. The video-parameter table test examines each of the parameter tables to ensure that the video modes supported by a VGA-compatible adapter are exactly the same as those supported by the IBM VGA. Because video monitors are highly dependent on the synchronization signals sent by the CRTC, any variation in those signals could cause a monitor designed for the IBM VGA to fail to work properly.

Parameter-save buffer. Another auxiliary BIOS data table, this buffer holds the current set of register values programmed into the VGA's graphics-controller palette and overscan registers. The parameter-save buffer test uses the BIOS functions to change those registers and then examines this table for proper updates.

Alternate-text character set. The VGA BIOS supports an alternate-text character-set definition area, which allows the definition of alternate character sets on a mode-by-mode basis. When a text video mode is selected that has an alternate character set defined for it, this table is used to load that character set automatically. The test for this operation selects an alternate character set for one text video mode and ensures the set is installed properly whenever that mode is selected. It also checks that the alternate character set is *not* used for other text modes.

Alternate-graphics character set. This area is a buffer that functions just as the text-character definition table; its

format, however, is slightly different. It is used for graphics rather than text modes. The format of the routines is the same as for the previous test.

Display-adapter combination table. The VGA provides explicit BIOS support for more than one video adapter in the system by using a display-adapter combination table. The table describes the list of legal display-adapter combinations available in the BIOS. The test of the display-adapter combination table checks this list for compatibility with the PS/2 VGA BIOS list. Because multiple display-adapter support is tied closely to a system-board graphics system, compatible VGA boards are not likely to support this table completely.

User-palette table. This data area provides a complete set of user overrides for combinations of attribute-controller and video-DAC registers. When this table is filled out and a new BIOS video mode is selected, the alternate user definitions for these registers are used instead of the ROM BIOS definitions. The test for the user-palette table programs the standard register set to produce a display that should be unreadable (black text on a black background). Then the user-palette table is loaded with an alternate video-parameter set and the mode is programmed again; the same text display then should become visible as white text on a blue background.

CRTC register table. The INT 1DH table, pointed to by interrupt vector 1DH, contains register values for programming the Motorola 6845 CRTC used on the MDA and the CGA. Although the VGA does not use a 6845 and ignores the values in this table at all times, the table is maintained for compatibility purposes. The test of the CRTC register table checks that the table used by a VGA-compatible adapter is the same as the table on the PS/2.

DETECTING CROSS PURPOSES

Although the BIOS-level tests cover all areas of text and alphanumeric support at a low level, the evaluation suite also includes a set of alphanumeric support tests that exercise those functions in combinations that most applications are likely to use. The intent of these tests is to check for any inconsistencies or incompatibilities among functions that work properly in isolation but conflict with each other during more sophisticated operations.

One test determines alternate-font support. The selection of alternate VGA fonts should be usable at the application level as well as at the level of DOS INT 21H text-output routines. This test exercises alternate ROM font selection through a variety of operations to determine how fully supported that alternate selection is.

The suite then tests cursor operation and emulation. The VGA BIOS cursor routines operate in one of two modes—standard or emulation. Because the size of the cursor is set through the BIOS by explicitly specifying its starting and ending scan lines, the position and size of the cursor depend on how many scan lines each row of text occupies on the display. For the 200-line CGA display, each row of 25-column text comprises 8 scan lines; when the EGA introduced a higher-resolution 350-line display, the number of scan lines per row increased to 14 for the same BIOS text modes. If an application sets an underline cursor on the CGA by setting the cursor to start on line 6 and end on line 7 (the scan-line numbering starts at 0), then on the EGA in the same mode the cursor would appear as a thin line in the middle of the character.

Register compatibility is the acid test because it means the hardware does not depend on an insulating layer of OEM BIOS.

To avoid this problem, the EGA and subsequently the VGA provide a cursor-emulation flag. If this flag is set, the BIOS assumes that the cursor size is being set based on an 8-line character cell; scan line 6, therefore, is not the seventh line of the cell but rather the scan line one up from the bottom. For a 14-line font, the BIOS translates a start-at-line-6 request for the cursor into a start-at-line-12 request.

The cursor emulation is turned on and off by a flag in the BIOS data area. The cursor-emulation tests check for proper positioning and sizing of the cursor for several character-cell heights with emulation enabled and disabled.

In addition to the ROM-based character sets supplied by the VGA, the BIOS supports the loading of user-defined custom-character sets that then behave exactly as the original sets. The test creates user-defined character sets by taking the ROM-based sets, copying them to local RAM, flipping the definition of each character so that the new character set is a mirror image of the original, and then informing the BIOS to start using that character set.

THE ACID TEST

Register compatibility is considered the acid test of VGA compatibility because it means the hardware provided on a given VGA does not depend on an insulating layer of OEM-developed BIOS or driver software to provide the functionality of IBM's VGA. Application software can take advantage of features provided in the original IBM VGA register set (see table 2). Because most commercial software does just that, register compatibility is the only kind of compatibility of practical interest to most users; if a given board does not meet this test, it is almost sure to fail to run some important applications.

The *PC Tech Journal* VGA evaluation suite covers register compatibility with the documented features of the IBM VGA system. It intentionally does not try to dig into the behavior of undocumented registers and reserved bits. Each of the following register tests exercises the behavior of one particular VGA register; because many of these registers control video output, tests for their proper behavior require visual confirmation of their effect. In general, however, these tests run in an automated manner and report errors as they are detected.

General registers. The VGA's general registers are not associated specifically with one of the VGA's major functional areas but instead control general I/O behavior of the VGA. The evaluation suite's general-register tests cover the operation of these registers as seen by applications and system-level software.

The general-register tests check for port-address selection (the VGA can appear at either monochrome or color adapter I/O addresses), synchronization-polarity status, and the values reported by the two input status registers. The feature-connector output bits in the feature-control register are not tested because these bits do nothing but drive the output state of two feature-connector pins and would require a hardware device connected to those pins to confirm their correct operation.

DAC-interface registers. Unlike earlier IBM video systems, the VGA uses a video DAC to display as many as 256 colors simultaneously from a palette of 262,144. The DAC-interface registers control the operation of the DAC and the selection of colors from it; this fine

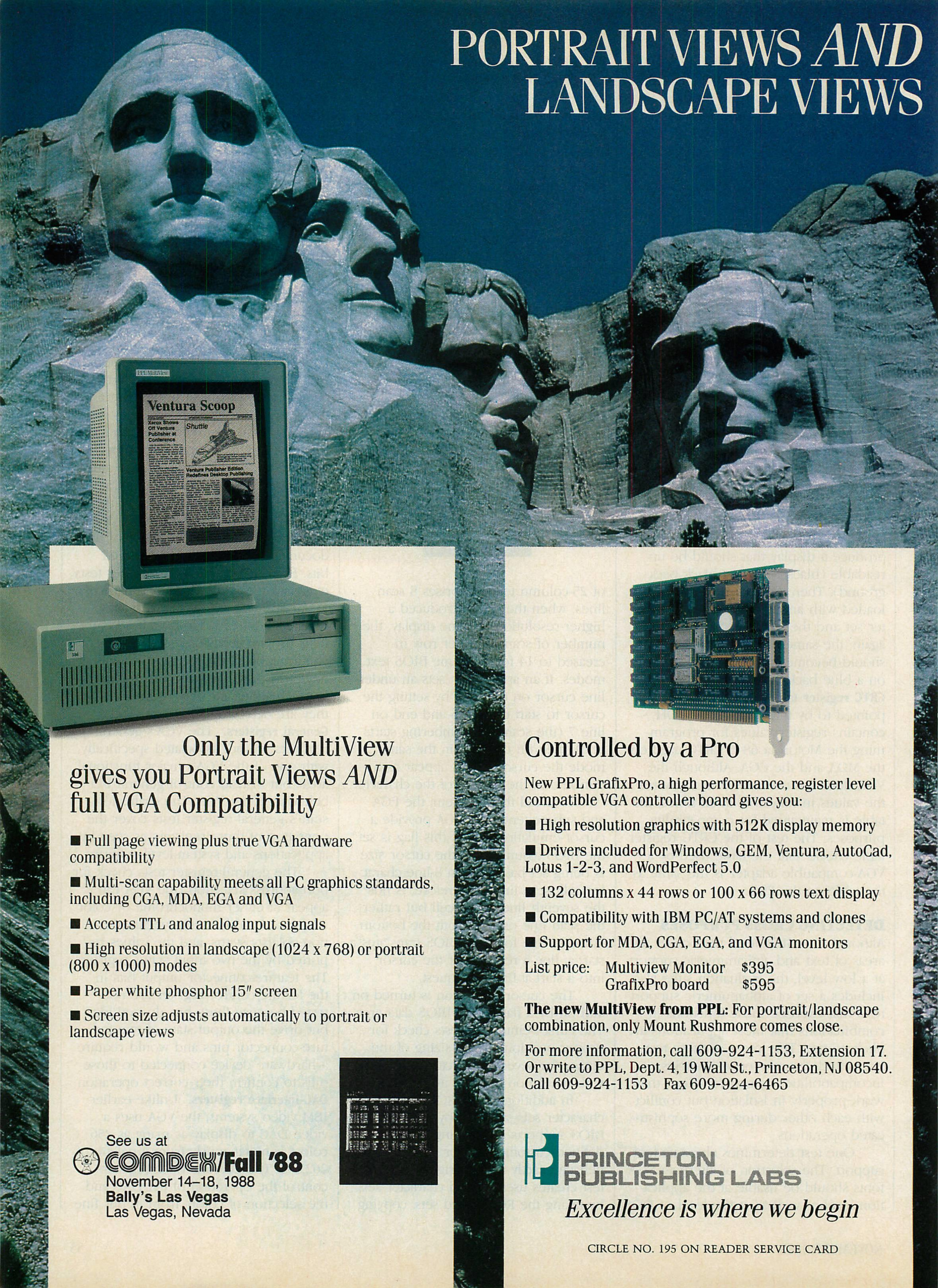
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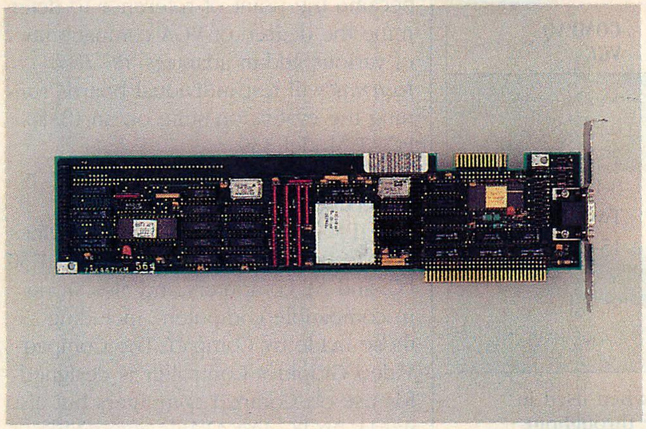
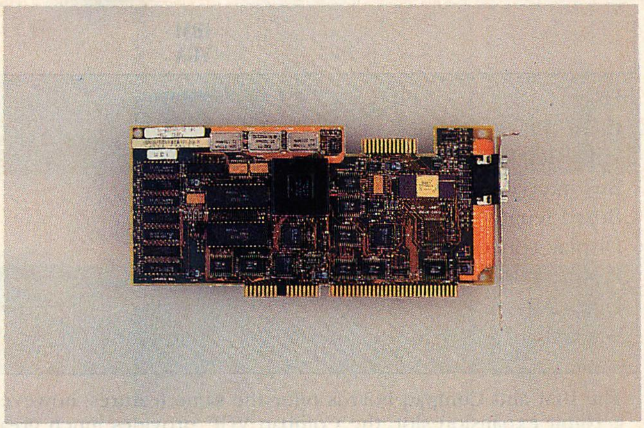
PHOTO 1: *IBM VGA Board*



The IBM VGA board is a standard full-length PC board, but with the smaller height of a Micro Channel board. It has the same chips that are used on the system-board VGA.

PHOTO 2: *Compaq VGC Board*



The two-thirds-length Compaq VGC board uses the Paradise VGA chip plus the same INMOS DAC as the IBM board, but it incorporates more surface-mount technology than IBM.

control over color output from a huge palette is a large advance over earlier EGA color support, and it represents a new level in compatibility requirements for manufacturers of VGA-compatible products.

The DAC interface is tested by setting and reading back each DAC translation value. Although this test alone does not guarantee the correct operation of the DAC interface, it is supplemented by visual confirmation that the colors being programmed produce desired output.

Sequencer registers. The VGA's sequencer performs actual memory control and coordination. Because the system CPU must be given read/write access to the VGA's display buffer at the same time the video-refresh circuitry is reading the display buffer to update the screen, the sequencer serializes and coordinates both operations. Errors in sequencer control-register support can cause incorrect CPU access to display memory and the corruption of video-display output.

The sequencer registers are tested by loading several character sets into the VGA's display memory and then using the sequencer to select among them while a block of text is displayed on the screen. The selection of the display of eight or nine pixels per byte also is tested, using the mode-setting commands. The remaining sequencer registers, including the map-mask register and the odd/even-address and chain-four-function bits in the memory-mode register, are used with the graphics-controller registers to perform display-memory reads and writes. They are tested in conjunction with the graphics-controller register tests.

CRTC registers. The CRTC provides all video-timing signals to control the display monitor connected to the VGA. Adjusting the CRTC registers supports new display resolutions and monitor configurations. Most applications software, however, does not need to use the synchronization-signal registers and is interested only in cursor-control and video-status reports. The set of synchronization-signal registers is by far the largest in the VGA, and it is difficult to test. Modifying these registers changes the VGA's synchronization signals.

These registers are not tested because special hardware other than the display is required to determine the accuracy of the results. If the display output is corrupted, it could be a result of an incorrect register setting or a monitor that is not capable of supporting the new video parameters. The BIOS mode-setting tests run through all legal combinations of video signals and should detect any significant failure of these registers.

The cursor scan-line start and end registers are tested by setting and reading back the cursor values, and the CRTC registers supporting panning and scrolling are exercised with visual confirmation of their operation. Finally, the VGA's vertical-interrupt feature is controlled by the CRTC. This feature is tested even though IBM has not implemented the feature on its VGA adapter board due to possible conflicts with other expansion boards.

Graphics-controller registers. The graphics-controller registers are usually of most interest to software developers because they provide the bulk of the drawing and memory-update support for the graphics system. This part of the evaluation suite is most thorough because of its crucial nature; any incompatibilities in the graphics controller almost certainly will result in applications software problems. Not only is the graphics controller's operation most critical to applications software, but also, by its very nature, it is easiest to test rigorously through software.

The evaluation suite's graphics-controller tests exercise every control bit in every register in this set, with the exception of the two-bit memory map flag, which determines the memory address of the display buffer. Because a given address assignment could conflict with other installed hardware, this test is omitted. In addition to testing the graphics-controller registers, this set of tests covers those sequencer registers that have functions related to drawing.

The graphics controller governs the CPU's access to writing and reading display memory. To confirm that every drawing operation performed by each combination of graphics-controller registers produces the correct pixel values in the display buffer, a set of tests runs through all the VGA's reading and writing modes. Because the graphics controller's drawing operation works independently of the BIOS video mode, these tests are run using mode 12H.

Attribute-controller registers. The attribute controller at I/O address 3C0H operates differently from the other subsystem register sets. Instead of having a paired-address and data register, these two registers share the same I/O address. By reading the attribute-controller register at address 3BAH or 3DAH, the register at 3C0H is set to address mode. Alternate writes to this register toggle between addresses and data.

TABLE 3: *VGA Board Features*

	IBM VGA	COMPAQ VGC
Price	$595	$599
BIOS data	10/27/86	02/17/88
Video RAM (KB)	256	256
Bus interface	8-bit	8/16-bit
Board length	Full	Two-thirds
Display connector	15-pin	15-pin
Feature connector	Standard	Standard
Diagnostics	Standard	Standard
Warranty	One year	One year

The IBM and Compaq boards offer the same features; however, when used in a 16-bit expansion slot, the Compaq VGC provides much greater throughput.

TABLE 4: *Compatibility Test Results*

	IBM		COMPAQ	
	Color	Monochrome	Color	Monochrome
BIOS				
Mode support	●	●	●	○[a]
Cursor operation	●	●	●	●
Light-pen support	●	●	●	●
Multiple pages	●	●	●	●
Screen scrolling	●	○[b]	●	○[b]
Text I/O	●	○[c]	○[d]	○[c]
Graphics I/O	●	●	●	●
Palette/DAC	●	●	●	●
Save/restore video state	●	●	●	●
Character generator	●	●	●	●
HARDWARE				
General registers	○[e]	○[f]	○[e]	●
DAC registers	●	●	●	○[g]
Sequencer registers	●	●	●	●
CRT controller registers	●	●	●	●
Graphics registers	●	●	●	●
Attribute registers	●	●	●	●

● = *Yes* ○ = *No*

[a] *Background not black in many modes; inconsistent behavior.*
[b] *Error in character/attribute for some modes.*
[c] *Mode D failed; Mode F succeeded when it should have failed.*
[d] *Incorrect colors in Mode 11.*
[e] *Reserved bits in ISR0 are for most modes.*
[f] *Reserved bits in ISR0 are for Mode 0.*
[g] *DAC table has errors.*

Neither board is completely compatible with the PS/2 system-board VGA. Also, the Compaq board's DAC table is slightly different in some monochrome modes.

The attribute controller regulates the programming of the VGA's palette registers as well as general mode-setting and color-output features of the VGA. Tests of the attribute controller exercise the operation of the palette registers in the same manner that the DAC registers are tested. The tests also cover the operation of the mode-control register as it affects display features and pixel panning.

Finally, the suite evaluates an adapter's compatibility with IBM's VGA split-screen and panning support (see "Pixel Panning and Split Screens," Richard Wilton, p. 62). A set of tests examines the operation of text split-screen support and the ability of the adapter to pan and scroll the video display over a larger image in the video buffer in both text and graphics modes.

Before testing individual boards, the entire VGA evaluation suite first was run on an IBM PS/2 Model 50, once with a color monitor and once with a monochrome monitor. The resulting baseline data and sets of register values for IBM's system-board VGA became the point of reference to determine the degree of VGA compatibility of various add-in adapters. *PC Tech Journal* will test individual boards running the evaluation suite on an IBM PC/AT Model 339.

IBM AND COMPAQ BOARDS

The IBM PS/2 Display Adapter provides VGA features to the IBM PS/2 Model 30, PC, and AT computers and also works in compatible computers, including those made by Compaq. The Compaq Video Graphics Controller is designed for use on Compaq computers but also works on PC and AT-bus compatible computers. The features of each board are summarized in table 3.

The IBM adapter is unusual in size, being a full-length PC-adapter board with the diminutive height of a Micro Channel board (see photo 1). It uses the IBM VGA and INMOS DAC chips used on the system-board VGA video system along with the standard 15-pin display connector. The top-mounted feature connector provides signals that the PS/2 system-board VGA provides on the Micro Channel video extension. IBM provides clear installation and testing instructions with the board along with diagnostics for use with IBM machines. A technical reference manual for the board is available at extra cost.

The Compaq VGC is a two-thirds-length board that uses the Paradise VGA chip and the same INMOS DAC as the IBM board, but it incorporates more surface-mount technology than IBM (see photo 2). It uses the same 15-pin display connector and top-mounted feature connector as IBM, but it has a full 16-bit expansion bus connector, rather than the IBM board's 8-bit connector. The Compaq board can be used in an 8-bit expansion slot but provides much faster performance when used in a 16-bit expansion slot. Two jumpers on the board indicate if it is to operate in, and if the video BIOS is to be accessed in, 8- or 16-bit mode. Accessing the BIOS in 16-bit mode generally provides better performance but may cause address conflicts with some LAN and expanded-memory boards. Compaq provides a diagnostics diskette and instructions for installing the board in its Portable III and Portable 386 as well as desktop computers. A technical reference manual is available at extra cost.

Table 4 shows the degree to which both the IBM and Compaq boards live up to the IBM system-board VGA. Nei-

ther board is completely compatible. The IBM adapter, when coupled with a color or monochrome display, duplicated the system-board VGA precisely except in one register—the general register set's input status register 0. That register's 5 and 6 bits were reserved and always read one on the VGA, but they read zero on the adapter. Because applications software should not depend on the value of reserved register fields, this incompatibility should not be a problem.

When using the IBM adapter on a monochrome display, a few additional problems arose in the BIOS tests, particularly those that used the BIOS to read characters from one position, write them to another, and then read them back again. When writing characters in video mode 0DH, some characters were written incorrectly in black, causing an attempt to read them back to fail. A similar problem caused the scrolling test to fail. Oddly enough, attempts to write black on black in video mode 0FH did not fail when they should have failed—the character was read back correctly when it should have been invisible.

The Compaq adapter showed identical errors on the BIOS text and scrolling routines when connected to a monochrome monitor, but it failed on a color monitor in video mode 11H. The input-status register's reserved bits also were set to 1 when a color monitor was attached, but attaching the monochrome monitor caused them to revert to their correct value of 0, unlike the IBM adapter.

Attaching a monochrome monitor and setting monochrome gray-scale modes caused the Compaq adapter to load a set of DAC-interface register values, which did not exactly match the PS/2 values when attached to the same monitor. The resulting discrepancy in gray scale caused some visual problems to appear during the BIOS-mode support test. Although all video modes could be programmed and appeared to work properly, some modes had a dark-gray background instead of a black one. This seemed to be only a cosmetic problem—the output was still readable, but the lack of a high-contrast background was disconcerting.

The performance of both boards was compared using the text scrolling, windows/scrolling, and 16-color graphics tests from the *PC Tech Journal* systems benchmark suite. As seen in table 5, the Compaq board, when used with its 16-bit interface and 16-bit BIOS mode, runs the text scrolling and windows/scrolling tests twice as fast as the IBM board with its 8-bit interface. The Compaq adapter board is only about 10 percent faster on the graphics test because the Microsoft C graphics routines used in the test do not take advantage of 16-bit I/O.

TABLE 5: ***Performance Test Results***

	IBM VGA	COMPAQ VGC
HLTEXT (text scrolling)		
BIOS	20.05	7.91
DOS	22.96	10.71
C library	20.49	8.73
Windowed	11.09	5.87
Total	74.61	33.24
HLWINDOW (window/scrolling)		
Total	15.98	7.74
HLGRAPH (16-color graphics)		
400 small areas	7.58	6.53
100 large areas	5.16	4.01
400 small ellipses	10.49	10.10
200 large ellipses	9.89	9.45
4,000 short lines	7.36	6.59
2,000 long lines	6.64	5.98
General graphs	1.70	1.53
Total	48.84	44.23

All times are in seconds, converted from 18.2-Hz timer ticks; therefore, total displayed is not always the exact sum of the individual results displayed.

The Compaq VGC board, with its 16-bit interface, performed the text scrolling and window/scrolling tests more than twice as fast as the 8-bit IBM VGA board.

Although neither the IBM nor the Compaq adapter made a 100-percent grade on these tests, neither failed in matters likely to be important to commercial applications. Some differences were cosmetic and some were situations in which an operation that should have failed succeeded. At $599, the Compaq adapter costs four dollars more than the IBM board but provides much greater performance and about the same degree of compatibility. As *PC Tech Journal* evaluates more VGA compatibles, these two candidates will provide a stern standard by which others can be judged.

MATCHING BEHAVIOR

Results of the evaluation suite should provide concise and valuable information to buyers and developers concerning the suitability of a given VGA system for their use. Broadly, VGA compatibility can be measured at the BIOS or the register level—BIOS compatibility will ensure that you can run DOS on your system but probably not much else (including OS/2).

Register compatibility by itself is much closer to the mark for most needs. The most significant features of the evaluation suite examine the operation of the VGA as a whole and how a compatible adapter's overall behavior matches that of the IBM system-board VGA video system.

Cooperative BIOS and register compatibility, high-level functionality, and consistent system behavior are the hallmarks of truly compatible VGA display adapters. As *PC Tech Journal* continues the evaluation of individual products, the greatest emphasis will be placed on this general compatibility—the level of quality and consistency that will allow applications software to run smoothly and allow users and buyers confidently to purchase and recommend compatible hardware for their daily requirements.

IBM Corporation
900 King Street
Rye Brook, NY 10573
800/IBM-2468; for nearest dealer, 800/447-4700
Personal System/2 Display Adapter
CIRCLE 338 ON READER SERVICE CARD

Compaq Computer Corporation
20555 FM 149
Houston, TX 77070
713/370-0670
Video Graphics Controller Board
CIRCLE 337 ON READER SERVICE CARD

Ed McNierney is a principal engineer at Lotus Development Corporation in Cambridge. Kent Quirk is president of Totel Systems Inc. in Westford, Massachusetts.

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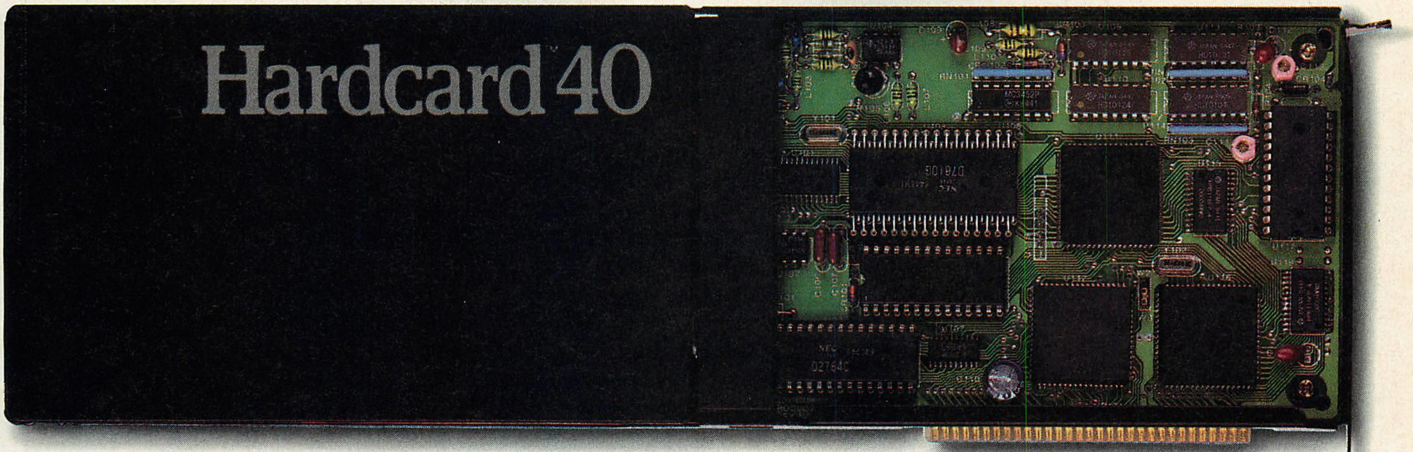

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Plus

Pixel Panning and Split Screens

Two overlooked virtues of the VGA allow easy access to parts of the picture outside the confines of the screen.

RICHARD WILTON

The Video Graphics Array (VGA) is more than just a huge, high-tech box of crayons with 256,000 brilliant hues and subtle shadings. Nor does its value to software and applications development end with the deep intensity with which its 640-by-480-pixel resolution can display colors on the screen. Contained within the VGA is hardware support for two features: pixel panning and split screens.

Pixel panning at the hardware level smoothly slides a screen image up, down, left, and right on the screen without the user having to wait for the software to redraw the image. Traditionally, most programmers have made graphics or text slide across the screen by copying blocks of characters or pixels from one location in the video buffer to another. VGA hardware, however, can do this cleaner and faster by moving part or all of the displayed image without the need for software to reshuffle pixels constantly.

Panning can save time in developing and using applications in which the video output normally extends beyond the confines of the screen and is especially important for applications that require users to access or monitor large amounts of data. For example, medical and scientific monitoring applications often require that the screen scroll constantly to the left to display recent input.

A split screen can display two separate parts of the video buffer simultaneously—one image on top, the other on the bottom. When using a split screen, commands and data entered in one part can update information automatically in the other. Thus, in a spreadsheet application, the user can input changes in one part of the screen and see them reflected in a chart on the other part of the same screen. This feature also could be used to develop a debugger that allows simultaneous viewing of outputs from the debugger and program being tested.

This hardware support for split-screen displays and pixel-by-pixel panning can be used for impressive demonstration programs as well as special effects. Practical applications that exploit these features are rare, however, because of the lack of support for VGA hardware in commonly used programming languages and libraries. As developers learn more about programming the VGA, this is likely to change.

The VGA's ROM BIOS does not directly support either panning or split-screen programming but instead supports repositioning the screen window in the video buffer. For example, INT 10H function 5 changes the value in the CRT controller (CRTC) start-address registers in increments of one full screen of text or graphics. IBM's ROM BIOS documentation refers to each screenful of data as a *display page*. This paged organization is no help for panning, but lets developers display data stored in otherwise unused portions of the video buffer.

Even though ROM BIOS support is lacking, you can develop applications that use hardware-level pixel panning and screen splitting without an enormous amount of programming. Routines presented in this article demonstrate how to redimension the video buffer to contain an unusually wide or long table, spreadsheet, or graph and then pan the screen window across all

ILLUSTRATION • ANDY LEVINE

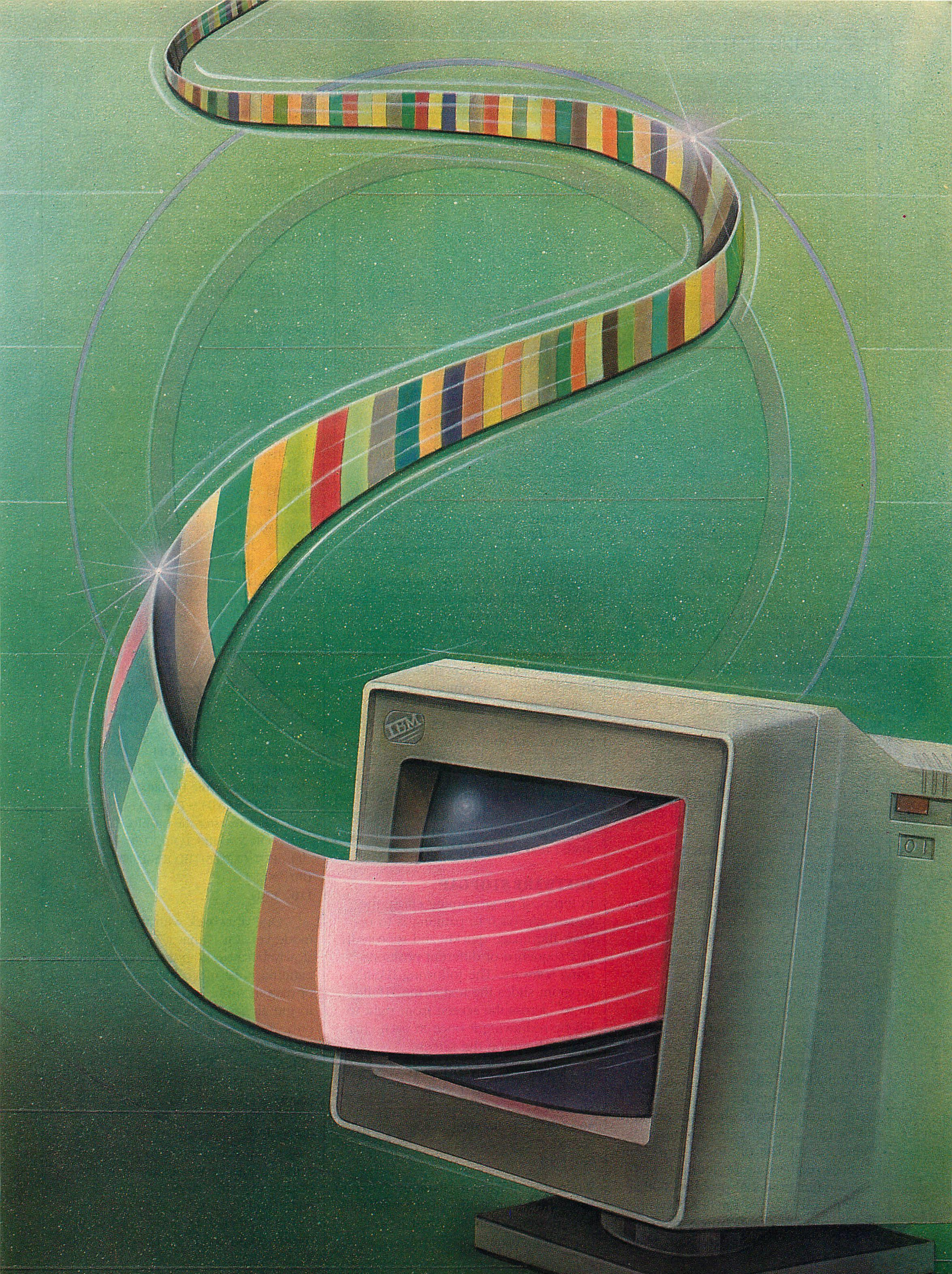
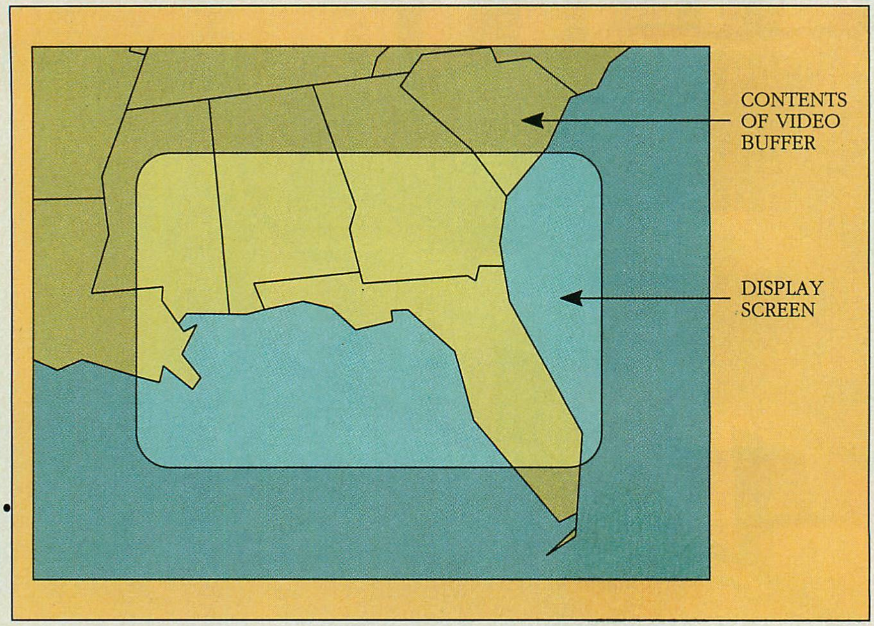

IBM
0 1

FIGURE 1: *VGA Display Screen*



The VGA display screen is a window on the contents of the video buffer; the screen boundaries delineate the visible portion of the data in the video buffer.

data in the video buffer. They also show how to add a split screen to maintain a caption in the lower part of the screen while panning the upper.

YELLOW FOR CAUTION

Although the panning and split-screen programming techniques for the VGA are comparatively straightforward, they illustrate some difficulties in video-hardware programming. Any program that relies on the VGA's hardware panning or the split-screen feature is not portable to video hardware that does not support it.

Many software developers have steered away from both of these features in the past because of lack of support from IBM's earliest PC-graphics standard, the Color Graphics Adapter (CGA). This is less an obstacle, however, now that the VGA is standard on new computer systems and the CGA is fading into the canvas.

Perhaps more annoying is the fact that some panning techniques for the VGA do not quite work on the Enhanced Graphics Adapter (EGA), which IBM introduced after the CGA and before the VGA. Both the EGA's CRTC and its attribute controller lack some of the functionality provided in the VGA. Therefore, the use of these features on the EGA requires more coding.

Another potential problem is that some non-IBM VGAs for PC/AT-compatible systems fail to offer the same panning or split-screen functionality as a true-blue VGA. All VGA features described in this article are documented by IBM, and all examples given should work on compatible VGA boards available from third parties. As an added safety measure, buyers may want to test these features on compatible boards before purchasing them.

Exploiting the VGA's support for panning and split-screen images is not an insurmountable problem. Learning how to make the most of these capabilities in both alphanumeric and graphics video modes is the key to developing applications that demand smoothly animated text and graphics.

SOFTWARE STOPGAP

In terms of programming effort, the easiest approach to panning is to redraw the image quickly and repeatedly in a sequence of different positions using software. The following BASIC program slides the text string "Hello, there" across the screen from right to left by redrawing it once in each character column on the screen:

```
10  SCREEN 0 : KEY OFF : CLS
20  FOR X = 60 TO 1 STEP -1
30  LOCATE 1,X,0
40  PRINT "Hello, there ";
50  NEXT
60  END
```

When this alphanumeric-mode program runs, the string seems to zip across the screen until it comes to rest in the upper-left corner.

The panning effect that this simple program produces is not particularly useful, however. The movement of the text string may appear smooth when the program runs at full speed, but slowing the rate at which the string slides across the screen—as is the case in most real-world applications—makes its movement appear increasingly jerky. (To demonstrate this problem, insert a delay loop between lines 30 and 40 of this program.)

The problem results because the distance between successive appearances of the string on the screen is the width of one character—about one-tenth of an inch on a typical VGA display. The human eye perceives this movement as a jerky motion rather than as smooth panning.

A reasonable solution is to move the string in increments of one pixel instead of one character. This is accomplished in software using one of the VGA's graphics modes. In alphanumeric mode, the string is positioned to the nearest character row or column; in graphics mode, the developer has more detailed pixel-by-pixel control over the string's location on the screen.

The following BASIC program illustrates how pixel-by-pixel panning in a graphics mode can appear much smoother than character-by-character panning in an alphanumeric mode:

```
10  DEFINT A-Z : DIM BITBLOCK(58)
20  REM 640 by 200 2-color graphics
30  SCREEN 2 : KEY OFF : CLS
40  LOCATE 1,61,0 : PRINT "Hello, there ";
50  REM Copy the bit block
60  GET (480,0) - (584,7),BITBLOCK
70  REM Transfer the bit block
80  FOR X = 480 TO 0 STEP -1
90  PUT (X,0),BITBLOCK,PSET
100 NEXT
110 END
```

One drawback with the graphics-mode version is that it runs more slowly because graphics-mode software panning must move many more bytes of data in order to translate an image. In the alphanumeric-mode program, only 26 bytes of data represent the "Hello, there" string in the video buffer. This includes one attribute byte for each character in the string and accounts for the trailing blank at the end of the string. In 640-by-200-pixel two-color graphics mode (which is invoked using SCREEN 2 in BASIC), the same string is represented in 104 bytes of data (13 characters times 8 bytes per character). Displaying the same string in the VGA's 640-by-480-pixel 16-color mode would require 832 bytes of data

(13 characters times 16 bytes per character times 4 bit planes).

The large amount of data movement in graphics-mode software panning limits its usefulness. The speed at which an image can appear to move across the VGA screen is limited by the speed of the computer's microprocessor. The larger the image, the more slowly it moves.

Furthermore, a CPU that is busy shuffling pixels in the video buffer is not doing any other work. In multitasking operating environments such as OS/2, using this method can mean slowing the execution of other tasks as well as making on-screen performance rather sluggish.

A related drawback is that a large image in graphics-mode software panning can take a long time to redraw, resulting in a perceptible lag between the time the top of the panned image moves across the screen and the time the bottom moves. This time lag can cause the image to smear or ripple; it is most evident with large images and relates directly to the speed of the microprocessor.

THE TRUE GRIT

Where software support results in slow and jerky panning, hardware support is quick and smooth. By manipulating a few VGA parameters, the developer can move displayed images directly and smoothly across the screen. The VGA hardware also allows splitting the displayed image horizontally into two independent images, one of which can be panned smoothly while the other remains stationary.

In order to understand how the VGA hardware supports both smooth panning and split-screen displays, visualize the relationship between the image that appears on the screen and all the data that are actually stored in the VGA's video buffer. The buffer, which contains all the data displayed on the screen, is large enough to contain much more than one screenful of data. This means that what appears on the screen may not be the entire image that is contained in the video buffer.

Imagine the screen to be a window on the contents of the video buffer (see figure 1). This window is not to be confused with the notion of a window in an environment such as Microsoft Windows, where a window represents a logical region in which a program generates its output. Instead, the screen window delineates the visible portion of the data contained in the video buffer.

TABLE 1: *Pixel Panning*

VALUE IN REGISTER	FIRST PIXEL DISPLAYED	
	8 PIXELS[a]	9 PIXELS[a]
0	0	1
1	1	2
2	2	3
3	3	4
4	4	5
5	5	6
6	6	7
7	7	8
8	N/A	0

N/A = Not applicable

[a] *Number of pixels displayed from each byte in the video buffer*

The starting pixel of the image is determined by the value in the horizontal-pel-panning register and the number of pixels displayed per byte.

Although the video buffer is addressed with a linear sequence of addresses, imagine the video buffer as two-dimensional, with a logical width that corresponds to the number of characters or pixels that can be displayed in each row on the screen. The key to understanding how screen splitting and panning work on the VGA is to realize that the screen window can be positioned to display any portion of the video buffer, or (in the case of screen splitting) to display two separate portions of the data in the buffer.

Nevertheless, virtually all VGA programs ignore the extra memory in the video buffer. They assume that the origin of the screen window coincides with the start of the video buffer, and that the logical width of the video buffer is the same as the logical width of the screen. In effect, the VGA's video buffer is longer than the displayed screen image. In order to use the extra RAM in the video buffer, developers must know how to program the VGA's control circuitry to change the origin of the screen window and the logical width of the video buffer. Most programmers accomplish this by writing short assembly-language subroutines that directly access the VGA hardware, but some of the work can be done through calls to the VGA's ROM BIOS. Both of these techniques are used in listings 1 through 8, provided below.

NEW BEGINNINGS

The screen window is repositioned by changing its origin in the video buffer. To accomplish this, you need to know how to program the VGA's CRTC, which is the portion of the VGA circuitry that synchronizes the display circuitry's accesses to the video buffer with the timing signals that control the sweep of the electron beam across the video display.

In effect, the CRTC locates the screen window by determining the address in the video buffer that corresponds to the origin (that is, the upper-left corner) of the screen. The CRTC also determines the logical width of the video buffer. The combination of these parameters determines what portion of the video buffer is displayed in the screen window.

The VGA's CRTC uses a set of 25 internal 8-bit registers to store a wide range of values that control the timing signals necessary to drive the video display. Among these registers are three—start-address high, start-address low, and offset—that specify the start address of the screen window and the logical width of the video buffer. The developer can change these values by updating the contents of the appropriate CRTC registers.

All of the VGA's CRTC registers are accessed using the 8-bit I/O port at 3D5H. To access the port, first write a register number (0 through 18H) to port 3D4H and then read or write port 3D5H to access the corresponding CRTC register. (In video modes 7 and 0FH, which emulate the EGA modes supported on IBM's 5151 monochrome display, the relevant port addresses are 3B4H and 3B5H.)

The subroutine shown in listing 1 reads the value in a VGA CRTC register. The corresponding routine in listing 2 writes a value to a VGA CRTC register. These routines are written in assembly language, but, in general, developers can accomplish the same task in high-level languages that support port I/O. For example, both the Microsoft C functions **outp** and **inp** and the BASIC functions INP and OUT can access CRTC registers.

Vertical positioning. Several CRTC registers control the position of the origin of the screen window. The easiest ones to use are the two start-address registers, numbered 0CH and 0DH. These two registers contain the 16-bit offset of the first displayed byte of data in the video buffer, with the high-order byte of the offset in register 0CH and the low-order byte in register 0DH. When you call the VGA ROM BIOS to set up a video mode, the offset in the start-address registers is set to zero, positioning the screen window by default at the start of the VGA's video buffer.

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TABLE 2: ***ROM BIOS Data Area Video Parameters***

ADDRESS	SIZE	DESCRIPTION
0040:004A	Word	Number of character columns per row
0040:004C	Word	Number of bytes in each video page
0040:004E	Word	Value in start-address registers
0040:0084	Byte	Number of displayed character rows minus 1

These values in the BIOS data segment should be updated whenever BIOS routines are used to manipulate data in the nondisplayed portion of the video buffer.

Changing the CRTC start-address value repositions the screen window in the video buffer. Consider what happens in the C program shown in listing 3, where the start-address value is incremented by 80 in successive iterations of a program loop each time a key is pressed. In 80-column alphanumeric video modes, each iteration causes the screen window's position to move down a row of characters.

In a graphics mode, the results are similar. The difference is that each row of data in the video buffer is one pixel high instead of one character high. The resulting vertical movement of the screen window is smoother than in alphanumeric modes.

What about pixel-by-pixel vertical scrolling in alphanumeric modes? To accomplish this, you need to locate the screen window not only at a particular row of characters, but also at a particular scan line within the topmost character row. The VGA's CRTC provides a way to do this through its preset-row-scan register (8). The value in the five low-order bits of this register is set to zero whenever the ROM BIOS is called to establish a video mode; changing this value changes the scan line at which the first row of characters is displayed. Thus, the combination of the start-address and preset-row-scan values locates the screen origin at a particular pixel *y*-coordinate.

For example, in the VGA's default 80-by-25-pixel 16-color alphanumeric mode, each character row contains 16 scan lines (that is, 16 pixels). To scroll smoothly, increment the preset-row-scan value from 0 through 15. To get to the next row of characters, increment the start-address registers and set the preset-row-scan value to zero.

Horizontal positioning. When experimenting with the CRTC's start-address registers, you will notice that gradually incrementing the value in these registers moves the screen origin to the right, character by character. As in vertical positioning, you must program an additional register in order to achieve pixel-by-pixel horizontal positioning of the screen window.

The register that controls pixel-by-pixel horizontal positioning is in the VGA's attribute controller. Like the CRTC, the attribute controller uses a set of 8-bit registers mapped to a single pair of I/O ports to control the display of data. The attribute controller, however, is more difficult to program than the CRTC because the VGA hardware uses the I/O port at 3C0H both to select a register number and to write data to the register. (This I/O port's function is controlled by a switch whose state is reset when a program reads a value from the VGA's input-status register at 3BAH or 3DAH.) To avoid these complications, rely on ROM BIOS INT 10H function 10H, which provides two subfunctions (7 and 0) that read and write any designated attribute-controller register.

You must program both the CRTC and the attribute controller in order to position the screen origin at a particular pixel in the horizontal direction. The attribute controller's horizontal-pel-panning register (13H) designates the starting pixel in the video-buffer byte specified by the CRTC start-address registers. The assembly-language routine shown in listing 4 uses these start-address registers to position the screen window at a specified pixel location in the video buffer.

Determining the value for the horizontal-pel-panning register is slightly involved because the VGA can display either eight or nine pixels for each byte in the video buffer, depending on the video mode in use. You can determine the number of displayed pixels per byte by examining the low-order bit of the clocking-mode register (1) in the VGA's sequencer (which provides basic timing for video memory). This register is examined by writing its register number (1) to I/O port 3C4H and then reading port 3C5H to retrieve the contents of the register. Whether the VGA is displaying eight or nine pixels per byte, you can use the information in table 1 to determine the horizontal-pel-panning value required to produce the desired image shift.

Listing 4 brings all these hardware programming techniques together in a single, C-callable subroutine that positions the screen window's origin at a specified pixel location. Developers can achieve smooth panning and scrolling effects simply by calling the routine within an iterative loop. For example, the C program in listing 5 uses the subroutine in listing 4 to scroll the screen window smoothly down and up by 100 pixels.

Rewriting this program to scroll the screen window horizontally instead of vertically reveals a problem. The logical width of the video buffer is the same as that of the screen window, so horizontal panning simply wraps the screen image around the screen. Increasing the logical width of the video buffer will allow the developer to scan any material that extends beyond the width of the screen.

RESHAPING THE BUFFER

The key to redimensioning the video buffer is the CRTC-offset register (13H). This register specifies the logical width of the video buffer, measured in 16-bit words (not bytes). In 80-column alphanumeric video modes, the logical line width is 80 bytes and the value in the offset register is 28H (40 decimal). In graphics modes, each byte has 8 displayed pixels. Thus, in modes having a horizontal resolution of 640 pixels, the offset register again contains 28H.

To change the VGA video buffer's logical width, simply update the CRTC-offset register. For example, you can double the logical width in 80-column alphanumeric modes by storing 50H (80 decimal) in the offset register. Modifying listing 5 to do this before panning allows horizontal panning to proceed across 160-character columns without wrapping.

When redimensioning the video buffer, be careful not to exceed its 64KB logical size. For example, in 640-by-480 graphics modes, the logical width of the video buffer should be no larger than 65,536 bytes per 480 lines, which equals about 136 bytes (68 words) per line. Larger values cause the displayed image to wrap from the top to the bottom of the screen.

To use the display screen as a window on a video buffer that contains more than one screenful of data, you can fill the entire VGA video buffer with displayable text or graphics data. Although only a portion of the contents

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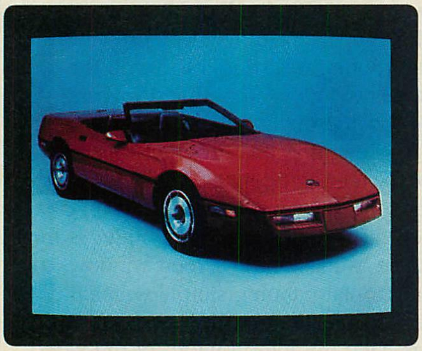

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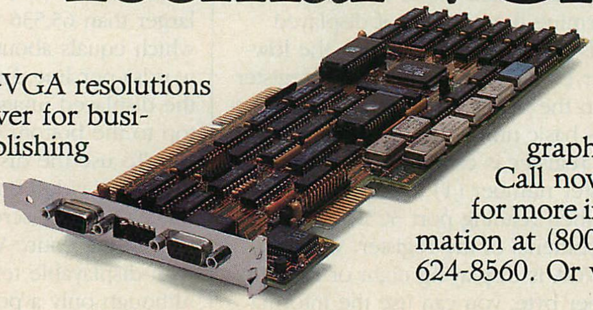

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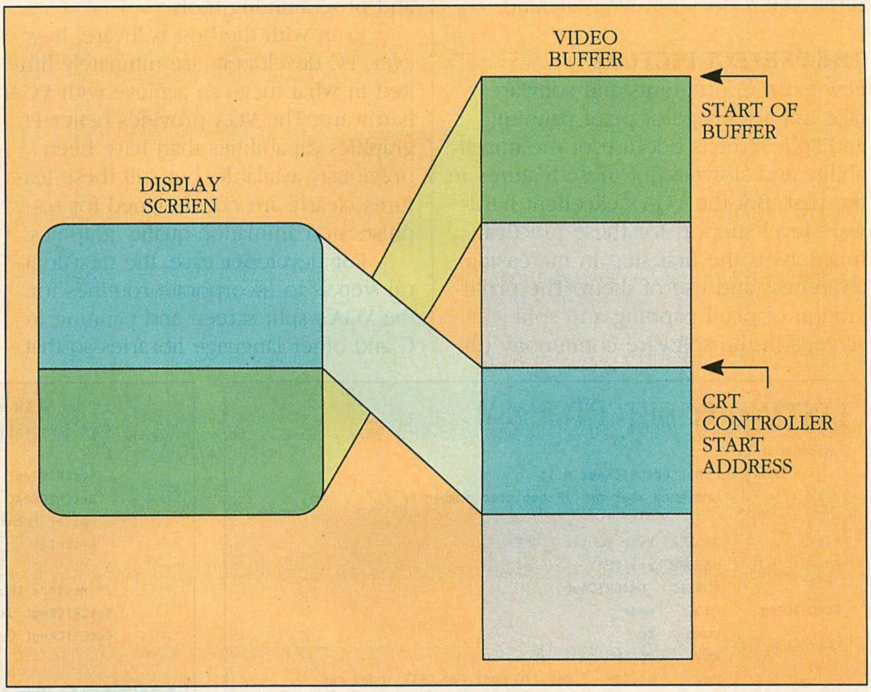
of the video buffer can be displayed at one time, you can arrange it so that keyboard commands or a pointing device will pan the screen to any desired location in the video buffer.

The ROM BIOS routines are comparatively tolerant about storing text or graphics data in nondisplayed portions of the video buffer. If you use the VGA ROM BIOS routines for this purpose, be sure to update the relevant status variables in the ROM BIOS data segment (see table 2). This helps ensure that the ROM BIOS INT 10H functions for character output (functions 9, 0AH, and 0EH) and pixel output (function 0CH) work properly.

FIGURE 2: ***VGA Split-screen Mode***



In split-screen mode, the VGA displays data from two different parts of the video buffer at the same time. The upper part of the screen displays data beginning at the video-buffer location specified by the CRTC start-address registers, and the lower part of the screen displays data beginning at the start of the video buffer.

SEPARATE BUT EQUAL

The VGA's split-screen display is essentially a display of two different portions of the video buffer at the same time. As shown in figure 2, the upper part of the video display contains the data from the portion of the video buffer designated by the CRTC start-address registers, and the lower part of the video display contains the data from the beginning of the video buffer (starting at offset 0 in the buffer).

When using the VGA split-screen feature, keep in mind that most commercial software packages use the beginning of the video buffer for output. This is the portion that appears in the bottom part of the split screen. For example, when using the DOS command processor, COMMAND.COM, the command-line prompt will appear in the bottom part of the screen. For data to appear in the top part of a split screen, you must store the data in the portion of the video buffer that begins at the address contained in the CRTC start-address registers.

You can change the size of the two parts of the split-screen display by specifying the scan line at which the split in the screen occurs in the CRTC line-compare register (18H). Like the other CRTC registers, line compare is an 8-bit register that contains a value no larger than FFH (255 decimal). Because the VGA can display more than 256 scan lines, the designers of the CRTC hardware had to find a way to let developers specify line-compare values larger than 255. They accomplished this by using a 10-bit line-compare value; bits 0–7 are stored in the line-compare register, bit 8 is stored as bit 4 in the CRTC overflow register (7), and bit 9 is stored as bit 6 in the CRTC maximum-scan-line register (9). Thus, in order to create a VGA split screen, you must update three different CRTC registers to store the 10-bit line-compare value (see listing 6).

To slide the split up and down (enlarging one or the other window), change the line-compare value within an iterative loop. Increasing the value enlarges the top part of the displayed image; decreasing the value expands the bottom part. To disable the split screen, use the maximum possible line-compare value (3FFH). This is the value used by default in all ROM BIOS video modes.

TWO-TONE PROGRAMS

Many developers combine panning and split-screen techniques in the same program only after they have developed routines for each feature separately and feel comfortable with them. When the two techniques are used together in one program, the result is that the bottom portion of a displayed image remains stationary while the top portion is moving.

The C program shown in listing 7 provides a simple example of how to accomplish this capability. The program produces the illusion of continuous output by plotting data points at the right side of the screen, panning from right to left, and then erasing all previously plotted points as they reach the left side of the screen. The assembly-language routine in listing 8 is used to set pixels on the screen.

A potential problem with split-screen panning can occur because changing the value in the horizontal-pel-panning register shifts both halves of the screen when developers most likely want to pan only one part. Developers can avoid this double panning by setting bit 5 of the attribute controller mode-control register (register 10H) to 1, which instructs the attribute controller to use a horizontal-pel-panning register value of zero for the bottom part of the split-screen image, regardless of the actual value. In listing 6, an INT 10H function is used to set bit 5 in the mode-control register so that all subsequent horizontal-panning operations will proceed smoothly.

This hardware solution, however, introduces a new problem—bad wrapping. In the default ROM BIOS alphanumeric modes, the VGA displays nine horizontal pixels per character. In this case, setting the horizontal-pel-panning register to zero shifts the displayed image left by one pixel as described in table 1. If the top part of the split screen is panned when the VGA alphanumeric mode is being used, the first-pixel column in the bottom portion of the split screen wraps from the left to the right side of the screen. Making the

first character blank in each line of the bottom part of the screen ensures that information does not wrap around.

THE PERFECT PICTURE

Few existing programs and software take full advantage of pixel panning and split screens because of the unreliability and slowness of these features in the past. But the VGA's excellent hardware-level support for these practical functions is the first step in increasing awareness and use of them. The proliferation of pixel panning and split screens in the software community can mean a new wave of increasingly functional and productive PC applications and programming tools.

Even with the best software, however, PC developers are ultimately limited in what they can achieve with VGA hardware. The VGA provides better PC graphics capabilities than have been previously available, but still these features clearly are not designed for sophisticated animation-quality graphics.

For developer ease, the next logical step is to incorporate routines for the VGA's split screen and panning in C and other language libraries so that developers do not have to re-create them. IBM and vendors of VGA compatibles would aid developers by supporting pixel panning and split screens at the VGA's BIOS level. This support would reduce the amount of assembly-language code developers must write to access these features.

Richard Wilton is a fellow in UCLA's Medical Informatics Program. He is author of the Programmer's Guide to PC and PS/2 Video Systems *(1987) and coauthor of* The New Peter Norton Programmer's Guide to the PC and PS/2 *(1988), both from Microsoft Press.*

LISTING 1: GETCRTCR.ASM

```
; Microsoft C:
;       unsigned char GetCRTCReg( n );
;               unsigned char n;  /* register number */
;
_TEXT           SEGMENT byte public 'CODE'
                ASSUME  cs:_TEXT
                PUBLIC  _GetCRTCReg
_GetCRTCReg     PROC    near
                push    bp
                mov     bp,sp
                mov     ax,40h  ; get I/O port for CRTC index reg
                mov     es,ax   ;  from ROM BIOS data area
                mov     dx,es:[63h]
                mov     al,[bp+4]  ; AL = register number
                cli             ; clear interrupts
                out     dx,al   ; write to CRTC index reg
                jmp     $+2
                inc     dx      ; DX = I/O port for CRTC data reg
                in      al,dx   ; AL = register value
                sti             ; enable interrupts
                xor     ah,ah   ; AX = return value
                pop     bp
                ret
_GetCRTCReg     ENDP
_TEXT           ENDS
                END
```

LISTING 2: SETCRTCR.ASM

```
; Microsoft C:
;       void SetCRTCReg( n, value );
;               int n;              /* register number */
;               unsigned char value; /* value to store in register */
;
_TEXT           SEGMENT byte public 'CODE'
                ASSUME  cs:_TEXT
                PUBLIC  _SetCRTCReg
_SetCRTCReg     PROC    near
                push    bp
                mov     bp,sp
                mov     ax,40h      ; get I/O port for CRTC index reg
                mov     es,ax       ;  from ROM BIOS data area
                mov     dx,es:[63h]
                mov     al,[bp+4]   ; AL = register number
                mov     ah,[bp+6]   ; AH = value
                out     dx,ax       ; store register number and value
                pop     bp
                ret
_SetCRTCReg     ENDP
_TEXT           ENDS
                END
```

LISTING 3: INCSTRTA.C

```
#include        <conio.h>
unsigned char SetCRTCReg( int, unsigned char );
main()
{
        int     i;
        /* increment the Start Address (CRTC registers OCH and ODH) */
        /*  by 80 in each loop iteration */
        for( i=0; i<=15; i++ )
        {
          SetCRTCReg( 0x0C, (80*i)>>8 );   /* high-order byte */
          SetCRTCReg( 0x0D, (80*i)&0xFF ); /* low-order byte */
          while( !kbhit() );               /* wait for a keypress */
          getch();
        }
        /* restore the screen origin to zero */
        SetCRTCReg( 0x0C, 0 );
        SetCRTCReg( 0x0D, 0 );
}
```

LISTING 4: SCREENOR.ASM

```
; Microsoft C:
;       void ScreenOrigin( x, y );
;               int     x, y;           /* pixel x,y coordinates */
;
_TEXT           SEGMENT byte public 'CODE'
                ASSUME  cs:_TEXT
                PUBLIC  _ScreenOrigin
_ScreenOrigin   PROC    near
                push    bp      ; preserve caller registers
                mov     bp,sp
; setup for pixel x-coordinate:
;     - determine 8 or 9 bits per pixel by examining bit 0 in
;         Sequencer Clocking Mode register
;     - compute value for Horizontal Pel Pan register
                mov     dx,3C4h ; DX = port for Sequencer index reg
                mov     al,1
                cli             ; disable interrupts
                out     dx,al   ; select Clocking Mode reg
                jmp     $+2     ; wait for Sequencer to respond
                inc     dx
                in      al,dx
                sti             ; set interrupts
                and     al,1    ; isolate low-order bit
                mov     cl,9
                sub     cl,al   ; CL = 8 or 9 (# of pixels/byte)
                mov     ax,[bp+4]       ; AX = pixel x-coordinate
                div     cl      ; AH = bit offset in byte
                                ; AL = byte offset in row
                cmp     cl,8
                je      L01     ; jump if 8 pixels/byte
                dec     ah      ; AH = -1, 0-7
                jns     L01     ; if AH = -1 ...
                mov     ah,8    ; ... set AH = 8
L01:            mov     cl,ah   ; CL = Horizontal Pel Pan value
                mov     bl,al
                xor     bh,bh   ; BX = byte offset in row
; setup for pixel y-coordinate:
;   - use value in CRTC Max Scan Line register to compute value
;       for CRTC Preset Row Scan register
;   - read CRTC Offset register to determine width of video buffer;
;       use this to compute value for CRTC Start Address registers
                mov     ax,40h
                mov     es,ax   ; ES -> video BIOS data segment
                mov     dx,es:[63h]     ; DX = port for CTRC index reg
                mov     al,9    ; AL = Max Scan Line reg number
                cli
                out     dx,al
```

```
        push    bx      ; preserve BX (byte offset in row)
        push    dx      ; preserve DX (CRTC index reg port)
        inc     dx
        in      al,dx   ; AL = Max Scan Line value
        sti
        and     ax,1Fh  ; AX = value from bits 0-4
        inc     ax
        mov     bx,ax   ; DX = scan lines per character
        xor     dx,dx
        mov     ax,[bp+6]       ; AX = pixel y-coordinate
        div     bx      ; AX = character row
                        ; DL = value for Preset Row Scan
        mov     ch,dl   ; save in CH
        mov     bx,ax   ; save character row in BX
        pop     dx      ; DX = port for CRTC index reg
        push    dx
        mov     al,13h  ; AL = Offset reg number
        cli             ; disable interrupts
        out     dx,al
        jmp     $+2
        inc     dx
        in      al,dx   ; AL = Offset reg value
        sti             ; enable interrupts
        xor     ah,ah
        mul     bx      ; AX = word offset of start of row
        shl     ax,1    ; AX = byte offset of start of row
        pop     dx      ; DX = port for CRTC index reg
        pop     bx      ; BX = byte offset in row
        add     bx,ax   ; BX = buffer offset
        add     dl,6    ; video status port (3BAH or 3DAH)
; update CRTC Start Address registers
L02:    in      al,dx   ; wait for vertical retrace
        test    al,8
        jz      L02
L03:    in      al,dx   ; wait for end of retrace
        test    al,8
        jnz     L03
        cli             ; disable interrupts
        sub     dl,6    ; DX = 3B4H or 3D4H
        mov     ah,bh   ; AH = Start Address High
        mov     al,0Ch  ; AL = Start Address High reg #
        out     dx,ax   ; update this register
        mov     ah,bl   ; AH = Start Address Low
        inc     al      ; AL = Start Address Low reg #
        out     dx,ax   ; update this register
        sti             ; enable interrupts
; update CRTC Preset Row Scan and
;  Attribute Controller Horizontal Pel Pan registers
        add     dl,6    ; DX = video status port
L04:    in      al,dx   ; wait for vertical retrace
        test    al,8
        jz      L04
        cli             ; disable interrupts
        sub     dl,6    ; DX = 3B4H or 3D4H
        mov     ah,ch   ; AH = value for Preset Row Scan reg
        mov     al,8    ; AL = Preset Row Scan reg number
        out     dx,ax   ; update this register

        mov     dl,0C0h ; DX = 3C0h (Attribute Cont. port)
        mov     al,13h OR 20h   ; AL bit 0-4 = Hor Pan reg #
                                ; AL bit 5 = 1
        out     dx,al   ; write Attribute Cont. Address reg
                        ;  (The Attribute Controller
                        ;    address flip-flop has been
                        ;    reset by the IN at L04.)
        mov     al,cl   ; AL = value for Horiz Pel Pan reg
        out     dx,al   ; update this register
        sti             ; re-enable interrupts
        mov     sp,bp
        pop     bp
        ret
_ScreenOrigin   ENDP
_TEXT   ENDS
        END
```

LISTING 5: SCROLLV.C

```
void ScreenOrigin( int, int );
main()
{
        int     y;
        for( y=0; y<100; y++ )          /* scroll down */
          ScreenOrigin( 0, y );
        for( y=100; y>=0; --y )         /* scroll up */
          ScreenOrigin( 0, y );
}
```

LISTING 6: SPLITSCR.ASM

```
; Microsoft C:
;       void SplitScreen( n );
;               int     n;      /* scan line at which */
;                               /*  to split screen */
;
_TEXT           SEGMENT byte public 'CODE'
                ASSUME  cs:_TEXT
                PUBLIC  _SplitScreen
_SplitScreen    PROC    near
                push    bp      ; preserve BP
                mov     bp,sp
                mov     ax,40h
                mov     es,ax   ; ES -> video BIOS data area
                mov     dx,es:[63h]  ; DX = port for CRTC index reg
; wait for vertical retrace
                add     dl,6    ; DX = 3BAH or 3DAH (status port)
L01:            in      al,dx   ; wait for end of vert. retrace
                test    al,8
                jnz     L01
L02:            in      al,dx   ; wait for start of vert. retrace
                test    al,8
                jz      L02
                sub     dl,6    ; DX = port for CRTC index reg
; isolate bits 0-7, bit 8, and bit 9 of the Line Compare value
                mov     ax,[bp+4]       ; AX = scan line value
                mov     bh,ah   ; BH bits 0-1 = bits 8-9 of
                                ;  Line Compare value
                mov     bl,bh
                and     bx,0201h  ; BH bit 1 = Line Compare bit 9
                                ; BL bit 0 = Line Compare bit 0
                mov     cl,4
                shl     bx,cl   ; BH bit 5 = Line Compare bit 9
                                ; BL bit 4 = Line Compare bit 8
                shl     bh,1    ; BH bit 6 = Line Compare bit 9
; update the CRTC registers
                mov     ah,al   ; AH = low-order 8 bits of value
                mov     al,18h  ; AL = Line Compare register number
                out     dx,ax   ; update Line Compare register
                mov     al,7    ; AL = Overflow register number
                cli
                out     dx,al
                inc     dx
                in      al,dx   ; AL = current Overflow reg value
                sti
                dec     dx
                mov     ah,al
                and     ah,11101111b    ; AH bit 4 = 0
                or      ah,bl   ; AH bit 4 = Line Compare bit 8
                mov     al,7    ; AL = Overflow register number
                out     dx,ax   ; update Overflow register
                mov     al,9    ; AL = Max Scan Line register #
                cli
                out     dx,al
                inc     dx
                in      al,dx   ; AL = current Max Scan Line value
                sti
                dec     dx
                mov     ah,al
                and     ah,10111111b    ; AH bit 6 = 0
                or      ah,bh   ; AH bit 6 = Line Compare bit 9
                mov     al,9    ; AL = Max Scan Line reg number
                out     dx,ax   ; update Max Scan Line register
; set bit 5 of the Attribute Controller Mode Control register
                mov     ax,1007h  ; AH = 10h (int 10H function #)
                                ; AL = 7 (subfunction number)
                mov     bl,10h  ; BL = Mode Control reg number
                int     10h     ; BH = Mode Control reg value
                or      bh,20h  ; set bit 5
                mov     ax,1000h  ; AH = 10h
                                ; AL = 0
                mov     bl,10h
```

```
                int     10h     ; update Mode Control register
                pop     bp      ; restore BP and exit
                ret
_SplitScreen    ENDP
_TEXT           ENDS
                END
```

LISTING 7: STRIPCH.C

```
#include        <stdio.h>       /* printf() */
#include        <math.h>        /* sin() */
#include        <dos.h>         /* int86() */
#define XEND    640
#define YEND    480
#define VPAGESIZE       ((XEND/8)*YEND)
void SplitScreen( int );
void ScreenOrigin( int, int );
void SetPixel( int, int, int, int );
void SetVideoMode( int );
union REGS      regs;   /* defined in DOS.H; used by int86() */
main()
{
        int                     i;
        int                     x,y;
        long                    lVBufOffset;
        unsigned char far *     lpVBufByte;
        unsigned int far *      lpCRT_LEN = (int far *)0x0040004C;
        /* select 640 by 480 16-color mode */
        SetVideoMode( 0x12 );
        printf( "This is 640 by 480 16-color graphics mode." );
        /* initialize video page 1 */
        printf( "\nDrawing grid lines in video page 1 ..." );
        *lpCRT_LEN = VPAGESIZE; /* update ROM BIOS variable */
        for(lVBufOffset=VPAGESIZE;lVBufOffset<0x10000L;lVBufOffset++)
        {
          lpVBufByte = (unsigned char far *)(0xA0000000L+lVBufOffset);
          *lpVBufByte = 0;                      /* zero all pixels */
        }
        for( x=0; x<XEND; x+=40 )       /* draw vertical lines */
          for( y=0; y<150; y++ )
            SetPixel( x, y, 1, 2 );  /* video page 1,pixel color 2 */
        /* split the screen */
        SplitScreen( 0 );
        ScreenOrigin( 0, YEND );
        printf( "\nSplitting .. " );
        for( y=1; y<=150; y++ )
          SplitScreen( y );
        /* draw a sine wave and pan to left while doing so */
        printf( "\nHorizontal Panning ..." );
        for( i=0; i<3; i++ )    /* do this for 3 screen widths */
        {
          for( x=1; x<=XEND; x++ )
          {
            if( i )             /* erase previously-drawn pixel */
            {
              y = 75 + (int)(75.0 * sin(0.03*(double)(x+(i-1)*XEND)));
              if( (x-1) % 40 )  /* use correct color for .. */
                SetPixel( x-1, y, 1, 0 );       /* .. vertical bars */
              else
                SetPixel( x-1, y, 1, 2 );
            }
            /* increment the screen origin (pan) */
              ScreenOrigin( x, YEND );
              /* set new pixel */
              y = 75 + (int)(75.0 * sin( 0.03*(double)(x+i*XEND) ) );
              SetPixel( x-1, y, 1, 7 );
            }
          }
          /* pan vertically, just to show how it looks */
          printf( "\nVertical Panning ..." );
          for( i=0; i<150; i++ )
            ScreenOrigin( 0, YEND+i );
          for( ; i>=0; --i )
            ScreenOrigin( 0, YEND+i );
          /* undo the split screen */
          printf( "\nUnsplitting .." );
          for( y=150; y>=0; --y )
            SplitScreen( y );
        ScreenOrigin( 0, 0 );
        SplitScreen( 0x3FF );
        printf( "\nDone." );
}
void SetVideoMode( mode )
int     mode;
{
        /* establish the specified ROM BIOS video mode */
        regs.h.ah = 0;
        regs.h.al = mode;
        int86( 0x10, &regs, &regs );
}
```

LISTING 8: SETPIXEL.ASM

```
; Microsoft C:
;
;               void SetPixel( x, y, v, n );
;               int x,y;        /* pixel coordinates */
;               int v;          /* video page (0 or 1) */
;               int n;          /* pixel value */
;
; Code based on routines in "Programmer's Guide to PC and PS/2 Video
; Systems" by Richard Wilton, published by Microsoft Press (1987).
;
_TEXT           SEGMENT byte public 'CODE'
                ASSUME  cs:_TEXT
                PUBLIC  _SetPixel
_SetPixel       PROC    near
                push    bp
                mov     bp,sp
; compute pixel address in video buffer
                mov     ax,80
                mul     word ptr [bp+6] ; AX = y*(bytes per scan line)
                mov     bx,[bp+4]       ; BX = x
                mov     cl,bl           ; CL = low-order word of x
                shr     bx,1
                shr     bx,1
                shr     bx,1            ; BX = x/8
                add     bx,ax           ; BX = y*(bytes per line)+x/8
                cmp     byte ptr [bp+8],0
                je      L01             ; jump if video page 0
                mov     ax,40h
                mov     es,ax           ; ES = BIOS data segment
                add     bx,es:[4Ch]     ; add CRT_LEN for video page 1
L01:            mov     ax,0A000h
                mov     es,ax           ; ES:BX = byte addr of pixel
                and     cl,7            ; CL = x & 7
                xor     cl,7            ; CL = # of bits to shift left
; set Graphics Controller write mode 2
                mov     dx,3CEh         ; GC address register port
                mov     ah,1            ; AH = unshifted bit mask
                shl     ah,cl           ; AH = bit mask in proper pos.
                mov     al,8            ; AL = Bit Mask register #
                out     dx,ax
                mov     ax,205h         ; AL = Mode register number
                out     dx,ax           ; AH = Write Mode 2(bits 0,1)
                                        ;      Read Mode 0 (bit 3)
                mov     ax,0003         ; AL = Function Select reg. #
                out     dx,ax           ; AH = read-modify-write bits
; set the pixel value
                mov     al,[bp+10]      ; AL = pixel value
                xchg    al,es:[bx]      ; rd-modify-write 4 bit planes
; restore default Graphics Controller register values
                mov     ax,0FF08h       ; default Bit Mask
                out     dx,ax
                mov     ax,0005         ; default Mode register
                out     dx,ax
                mov     ax,0003         ; default Function Select
                out     dx,ax
                mov     sp,bp           ; restore stack frame & return
                pop     bp
                ret
_SetPixel       ENDP
_TEXT           ENDS
                END
```

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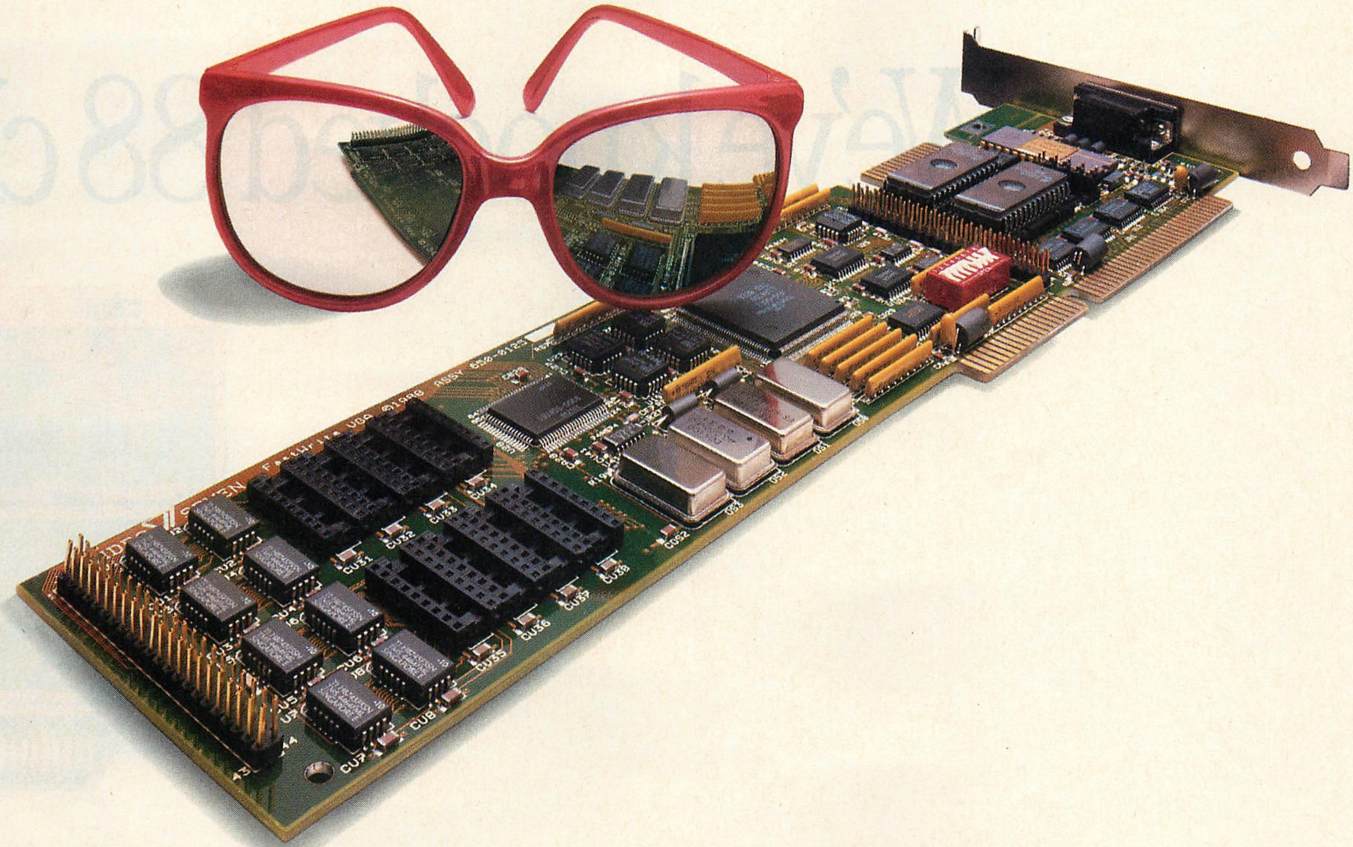

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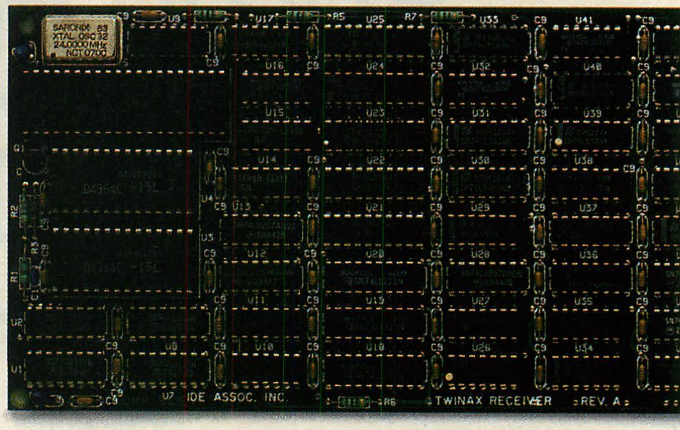

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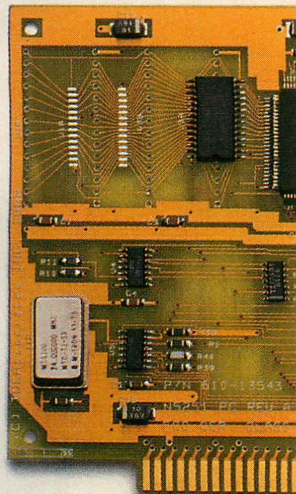

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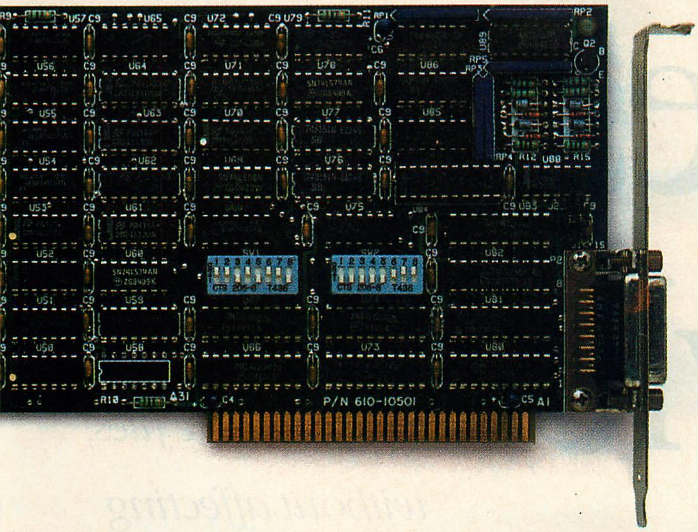

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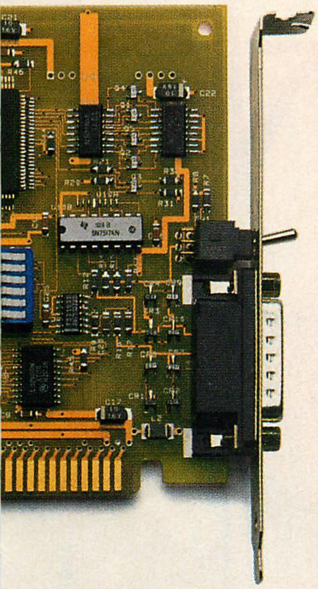

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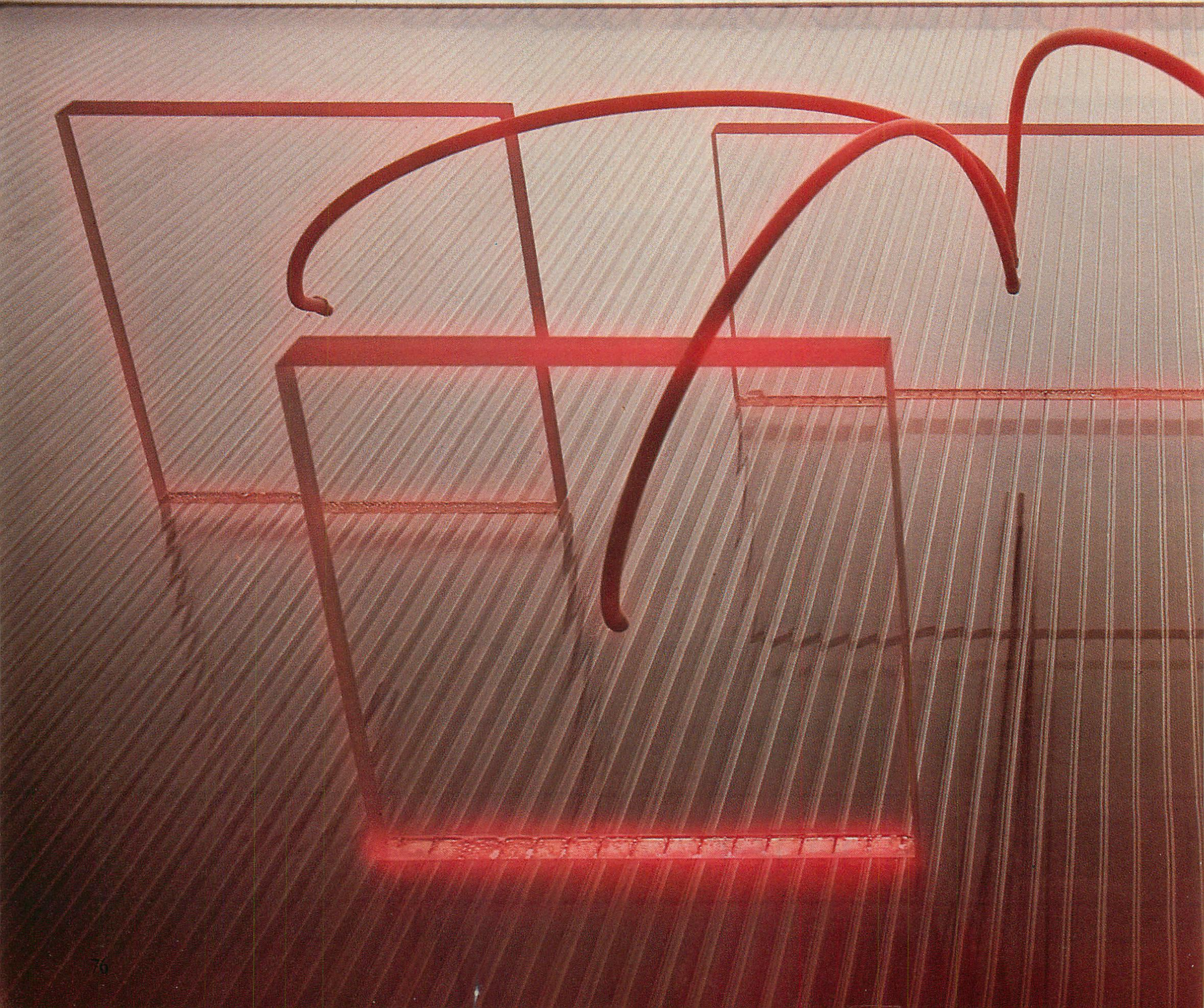
.EXE Files, OS/2 Style

The new capabilities of OS/2—memory protection and dynamic linking—require changes to executable files, without affecting DOS compatibility.

DAVID A. SCHMITT



OS/2 asks the developer for more than DOS does because it has more to do and it gives more back—more detailed processing and performance. Besides the obvious OS/2 advantages, file-structure compatibility between the two environments is a big plus, but it means that development in OS/2 is more complex. New OS/2 features require major additions to the executable (.EXE) file structure, but OS/2 family mode requires that these changes be made such that the same .EXE file is acceptable to both DOS and OS/2. (A family-mode application is one that runs under either environment—see "Family Ties," David A. Schmitt, June 1988, p. 124.)

An OS/2 application consists of one or more *processes* that are started by the user or by another process. In the OS/2 architecture, a process is an entity that owns system resources, such as memory, files, and mechanisms of interprocess communication, including semaphores, pipes, and queues. Once it is running, a process obtains and releases these system resources dynamically by calling appropriate application program interface (API) functions. An .EXE file specifies the initial set of memory resources necessary to start the process.

Under both DOS and OS/2, the system loader allocates physical memory space, loads code and data segments from the .EXE file, and adjusts memory references to reflect the program's actual location. However, OS/2 must do considerable additional work, as a consequence of its memory protection and dynamic-linking capabilities.

Memory protection limits the address space of a process to only the segments defined in that process. A program references memory not by means of physical segment addresses, but indirectly through segment descriptor entries in the local descriptor table (LDT). A descriptor defines the segment's physical location, length, type, and privileges. (See the sidebar "How Protected Mode Protects" in "An Architecture for the Future," Martin Heller, November 1987, p. 66.) The OS/2 loader constructs the LDT on the basis of information in the .EXE file.

Dynamic linking allows a program to call procedures that are not part of the program's .EXE file, but are loaded from other executable files called dynamic link libraries (DLLs). (See "OS/2's Dynamic Link," Mary DeWolf

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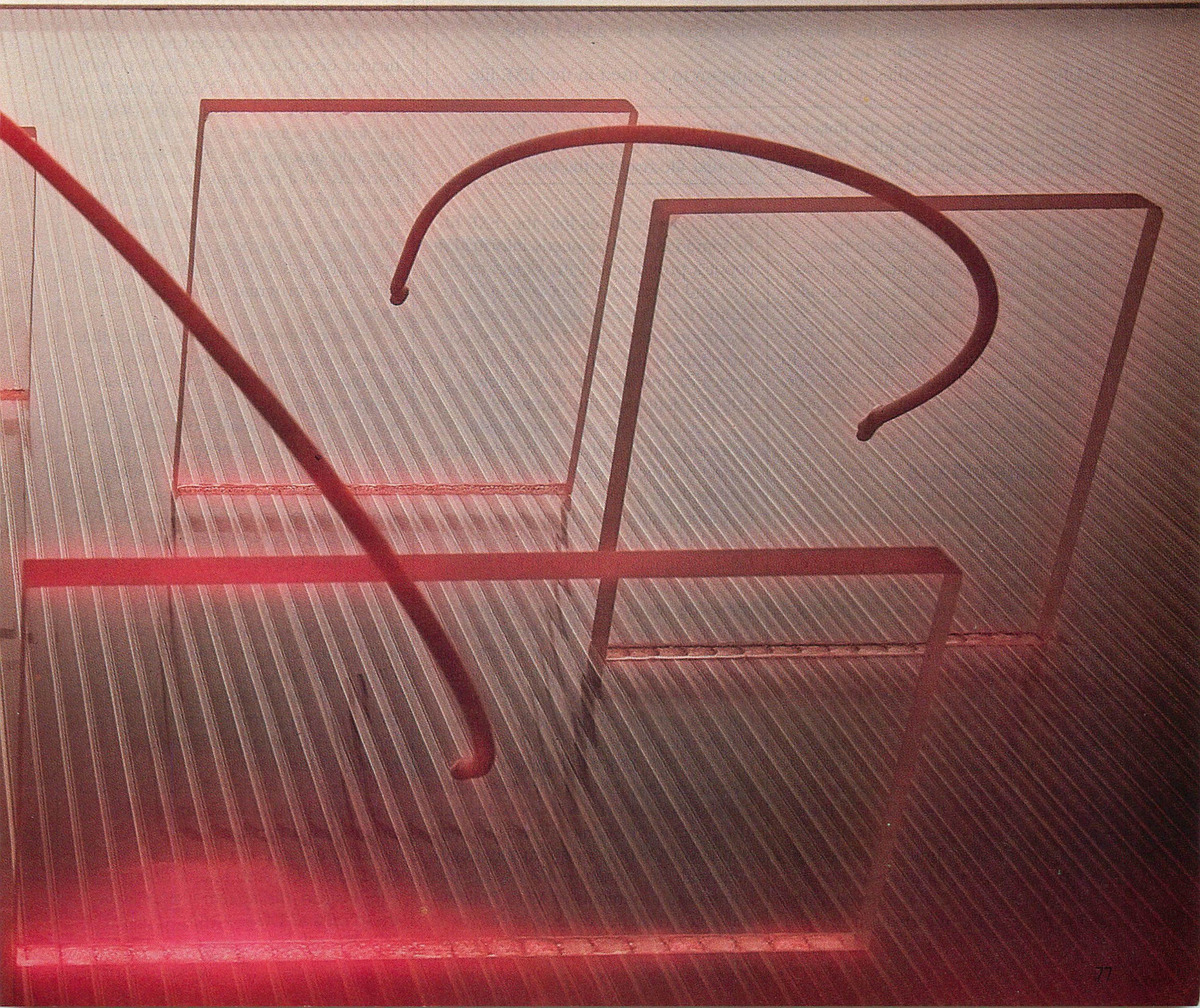


TABLE 1: ***Module Definition File Statements***

STATEMENT	DESCRIPTION
CODE	Defines default attributes of code segments, such as readability and I/O privileges.
DATA	Defines default attributes of data segments, such as writeability and shareability.
DESCRIPTION	Supplies a description, which becomes the first item in the nonresident name table.
EXPORTS	Defines symbols to be exported and specifies whether exportation is by name or by ordinal number.
HEAPSIZE	Defines the amount of heap space to be added to the default data segment.
IMPORTS	Defines functions that are imported from dynamic link libraries (DLL).
LIBRARY	Specifies that the linker should produce a DLL file instead of a stand-alone program file.
NAME	Defines the module name, which becomes the first item in the resident name table.
OLD	Specifies preservation of old ordinal numbers when rebuilding a DLL.
PROTMODE	Declares that the program can be run only in OS/2 protected mode.
SEGMENTS	Defines attributes of code and data segments on an individual basis.
STACKSIZE	Defines the amount of stack space to be added to the default data segment.
STUB	Specifies a DOS stub program to be used in the .EXE file.

To build an OS/2 .EXE file, the linker needs more information than can be specified in object and library files. The programmer supplies this type of additional information by means of these statements in a text file read by the linker.

and Ted Mirecki, September 1988, p. 100.) For load-time dynamic links, the OS/2 loader locates the called procedures, loads them if they are not already resident, and adjusts the program's call instructions to point to the appropriate locations within the DLL. In call-time dynamic linking, the OS/2 kernel performs these services at the calling program's request.

DEMANDING DETAILS

OS/2 requires many details about the program's structure to perform these functions. Such details are not necessary under DOS because DOS does not provide memory protection. DOS merely loads all segments of a program into a contiguous memory area—the loader needs no information about segment boundaries. The bulk of a DOS .EXE file is simply an image of this area. Moreover, DOS supports only static linking, which means that all called routines are in the same .EXE file and their addresses are inserted at link time, obviating the need for information to support load-time linking.

When the OS/2 linker processes object modules and libraries to construct the program file, it automatically inserts most of the information that the OS/2 loader requires into the .EXE file. In some cases, OS/2 needs information about a program that the object modules and libraries do not contain. You supply this to the linker via a *module definition file*; the OS/2 linker expects the name of the definition file after the names of link-time libraries. Table 1 lists the definition file statements.

Because OS/2 needs so much more information than DOS, you might expect a radically different and incompatible .EXE format. However, the need to support family-mode applications placed interesting constraints on the OS/2 designers as they defined the new, segmented executable format. The opposing requirements are handled by putting two separate programs into the OS/2 executable file, one for DOS and the other for OS/2, as shown in figure 1. This structure is not new to OS/2 but was developed originally for Microsoft Windows programs.

An OS/2 .EXE file begins with a DOS-formatted .EXE header (see table 2). The first 28 bytes, offsets 0 through 1BH, contain the same information as a standard DOS-only program file, beginning with the signature *MZ* (by his own admission, the initials of Mark Zbikowski, a key designer of DOS at Microsoft). Fortunately, the original header design was flexible enough to allow the expansion necessary to accommodate Windows and OS/2.

Information following the header occurs not at fixed offsets but at locations given by pointers within the header. For OS/2, the header is expanded to 64 bytes, and its last four words comprise a double-word pointer to the OS/2 portion of the file. A DOS relocation table, if one exists, follows the formatted header. A detailed description of the table format and relocation process can be found in the *DOS Technical Reference*.

The DOS application program follows the relocation table. Its position in the file is given by the header size (from the word at offset 8) multiplied by 16. The length of the program image in the file is determined by the following computation:

Program length = ((file pages − 1) * 512) + last page size − (header size * 16).

The file size encoded in the DOS header describes only the DOS portion of the file, up to the OS/2 header. If an OS/2 .EXE file is loaded under DOS, the loader is aware of only the front part and ignores the OS/2-formatted portions. In a program meant for protected-mode execution only, the DOS program is a short stub generated by the linker. Its purpose is to exit to the operating system after issuing the message, "This program cannot be run in DOS mode."

Some protected-mode utilities that come with OS/2 1.0 issue a "Program too big to fit" message when you attempt to run them under DOS. This happens because early versions of the OS/2 linker (which were distributed with the first Microsoft OS/2 Software Development Kit) did not insert a DOS stub program into protected-mode .EXE files. Instead, these linkers wrote an impossibly large (1MB) memory request into the word at offset 0AH of the header. DOS cannot load such a program because at best only about half that much free memory is available in real mode.

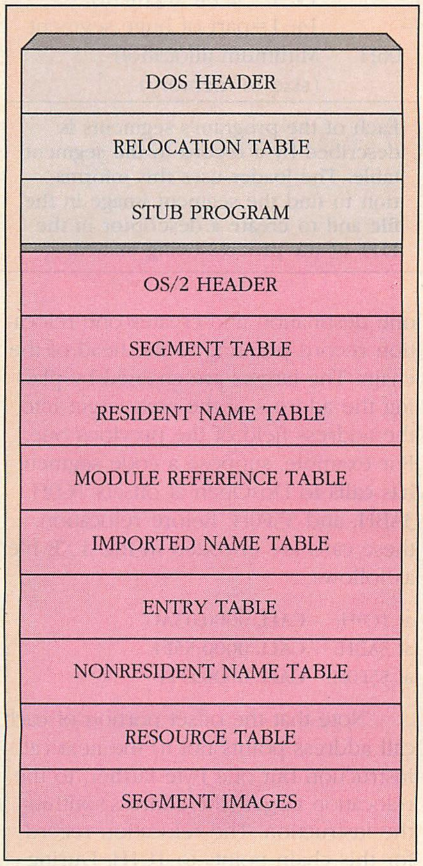
For a family-mode application, the DOS stub program is much more ambitious. This program contains the interface routines that provide real-mode equivalents of family API functions and a stub loader that reads in the OS/2 program and patches its API calls to point to the interface routines. Under OS/2, the DOS stub loader does not run; instead, the system loader links these calls to DLLs.

TABLE 2: *DOS Header Portion of OS/2 .EXE File*

OFFSET	LENGTH	DESCRIPTION
00H	2 bytes	Signature *MZ*
02H	Word	Bytes in last page of file
04H	Word	Number of 512-byte pages
06H	Word	Number of relocation items
08H	Word	Header size, in paragraphs
0AH	Word	Minimum additional allocation
0CH	Word	Maximum additional allocation
0EH	Dword	Initial SS:SP value
12H	Word	Checksum of entire file
14H	Dword	Initial CS:IP value (entry point)
18H	Word	Offset of relocation table from start of file
1AH	Word	Overlay number (0 for root overlay)
1CH	32 bytes	Reserved
3CH	Dword	Pointer to OS/2 .EXE header

Although the DOS header has been extended to 64 bytes, the first 28 bytes contain the same information as for a DOS-only file. Except for the last 4 bytes (ignored by the DOS loader), this header describes only the DOS portion of the file. OS/2 recognizes a protected-mode file by the position of the relocation tables.

FIGURE 1: *OS/2 .EXE File*



The head of the file is in DOS format, allowing the older operating system to load and run family-mode applications. The latter portion, read by OS/2 only, contains data structures in support of OS/2's enhancements: memory protection and dynamic linking. OS/2 uses the same format for both stand-alone programs and DLLs.

If the beginning of an OS/2 .EXE file is in DOS format, how does the OS/2 loader distinguish between DOS-only and OS/2 executables? First, it looks at the pointer to the DOS relocation table. An OS/2 file has the value 40H, a DOS file a value less than 20H. If the value is 40H, the loader looks at offset 3CH of the DOS header for a double-word pointer to the OS/2 header. If the pointer value is greater than 40H and less than the file length, the loader checks the target location for the OS/2 .EXE signature of *NE*—which stands for new executable.

The probability that a DOS .EXE file passes all these tests is infinitesimal, but to guard against even this chance, the loader assumes it is handling a DOS file if the information following the signature is in any way inconsistent—for example, if any pointers point past the end of the file. The OS/2 header has a cyclic redundancy check (CRC) checksum, but the loader does not use it to test file integrity.

TABLES IN TURN

As figure 1 shows, the OS/2 portion of the .EXE file consists of a header, a set of tables, and the code and data for loading into the initially allocated set of segments. The header (see table 3 and figure 2) gives overall information about the program and the locations of the various tables in the file. (Note: The header layout given in Appendix E of the *Programmer's Reference* in Microsoft's OS/2 Programmer's Toolkit is in error; table 3 gives the correct amount.)

The complexity of this structure is due primarily to its support of dynamic linking. The tables contain information that allows the linker to locate and load the DLLs that the program calls, and to patch the location of those routines into the call instructions. Furthermore, OS/2 has the same .EXE format for stand-alone programs and DLLs, and some of the tables provide the information about the exported entry points that can be dynamically linked to other programs.

The tables are discussed here not in the order they appear in the .EXE file but in an order that facilitates explaining the purpose and function of each. The order as given in figure 1 is not guaranteed for future versions of OS/2, and if you need to process the various tables in an .EXE file, you should always locate them through the position information in the header.

Segment table. For each code and data segment in the program, the segment table contains an eight-byte record in the format shown in table 4. The word at header offset 22H gives the location of the start of the table, and the word at offset 1CH gives the number of records. The ordinal position of each record in the table assigns a number to each segment: the first record identifies segment number 1, the second identifies segment number 2, and so on.

The .EXE header and the other tables use these numbers to identify the segments in the program. For example, if the entry-point segment (in the word at offset 16H of the OS/2 .EXE header) is n, then the nth record of the segment table defines the code segment containing the program's entry point. Although the number of segments is recorded in a word in the header, most of the other tables record segment numbers in a single byte, which results in a limit of 255 segments per program.

The OS/2 loader creates an LDT entry from each segment table record. The segment's privilege level and size are established, respectively, from the information in words at offsets 4 and 6 of the record. The first word gives the *logical sector number* in the .EXE file of the code or data to be loaded into the segment; if that word is zero, the entire segment is uninitialized. Otherwise, the loader calculates the byte offset in the file by shifting the record number left by the *segment alignment shift count* in word 32H of the .EXE header. By default, that value is 9, indicating that segments begin at multiples of 2^9 (512 bytes).

TABLE 3: *OS/2 .EXE Header Format*

OFFSET	LENGTH	DESCRIPTION
00H	2 bytes	Signature *NE*
02H	2 bytes	Version of linker that created this file
04H	Word	Offset from header of entry table
06H	Word	Entry table size
08H	Dword	32-bit checksum of the entire file
0CH	Word	Flags (see figure 2)
0EH	Word	Segment number of automatic data segment
10H	Word	Initial heap allocation, bytes
12H	Word	Initial stack allocation, bytes
14H	Word	Initial instruction pointer (IP) value
16H	Word	Segment number containing entry point
18H	Word	Initial stack pointer (SP) value
1AH	Word	Segment number of initial stack segment
1CH	Word	Number of segments in the program
1EH	Word	Number of entries in module reference table
20H	Word	Size, in bytes, of nonresident name table
22H	Word	Offset from header of segment table
24H	Word	Offset from header of resource table
26H	Word	Offset from header of resident name table
28H	Word	Offset from header of module reference table
2AH	Word	Offset from header of imported names table
2CH	Dword	Offset from start of file of nonresident names table
30H	Word	Number of movable entry points
32H	Word	Segment alignment shift count
34H	Word	Number of entries in resource table
36H	10 bytes	Reserved

As in DOS, the .EXE header in OS/2 provides information that the loader uses to load the program and prepare it for execution. The greater complexity arises from the need to create segment descriptor tables in protected memory and to establish load-time dynamic links to procedures in external files.

TABLE 4: *Segment Table*

OFFSET	DESCRIPTION
00H	Segment position within file
02H	Segment length in file (0=65,535 bytes)
04H	Flag bits: 0: 0=code, 1=data 3: 1=iterated data (see text) 4: 0=fixed 1=movable segment 5: 1=pure (sharable) segment 6: 0=load on call 1=preload 7: 1=execute-only code or read-only data 8: 1=segment has relocation information 9: 1=segment has debugging information 10–11: descriptor privilege level 12: 1=discardable segment 13: 1=32-bit segment 14: 1=part of huge segment
06H	Minimum allocation (size in memory)

Each of the program's segments is described by a record in the segment table. The loader uses this information to find the segment image in the file and to create a descriptor in the LDT of the process being loaded.

If bit 3 of the segment flag word indicates noniterated data, the loader simply reads into memory the number of bytes equal to the segment length on file (given by the word at offset 2 of the segment record). Iterated data specify how to initialize a segment with a pattern. The first word of an iterated segment specifies the number of iterations, the second gives the length of the pattern, and the next *n* bytes gives the pattern. For example, a 512-byte segment filled with the pattern 12H 34H is represented as:

```
0100 0002 12 34
```

The amount of data read from the file or generated by iterating a pattern can be less than the size of the segment. The difference represents an uninitialized portion of the segment that the loader sets to zeroes. Because such automatically zeroed data areas occur only at the high end of segments, a programmer can improve the efficiency of .EXE files by coding all uninitialized and zero values after nonzero ones.

Relocation. If bit 8 of the segment flag word indicates the segment has relocation data, OS/2 finds that data immediately after the segment image. Whereas a DOS .EXE file contains one relocation table, an OS/2 file has a separate relocation section for each segment.

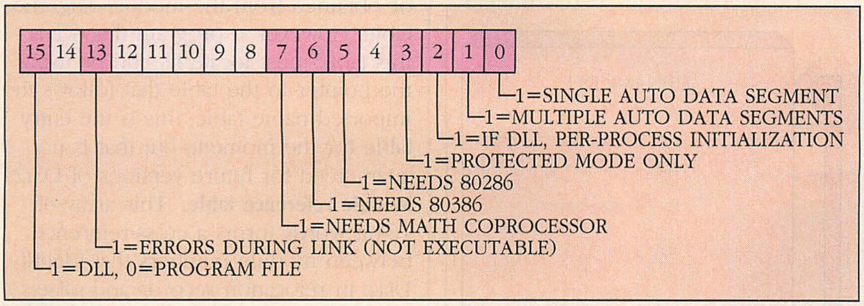
If relocation data exist, the first word after the segment image indicates the number of relocation records for that segment. As table 5 shows, each record is eight-bytes long and identifies two items. The first, the *relocation target*, points to a location in this .EXE file that contains a reference to an external location whose address could not be established at link time. The second, the *destination*, is the location referred to by the target; it can be a location in another segment of the same program or a procedure in a DLL.

A program typically contains many references to a particular external address. To save space, the OS/2 .EXE file does not need a separate relocation record for each such reference. Instead, the linker chains together all the targets in one segment that refer to one destination and creates one relocation record pointing to the head of the chain. The targets are chained by placing the address of the next target into the address field of the previous one. For example, suppose a code segment has calls to DosOpen at offsets 1C0H, 3ABH, and 55F0H. Before relocation, these calls are encoded in the .EXE file as follows:

```
at 1C0H:   CALL 0000:03AC
at 3ABH:   CALL 0000:55F1
at 55F0H:  CALL 0000:FFFF
```

Note that the offset portion of each call address points not to the next call instruction but one byte farther, to the relocation target (the address) within the instruction. The relocation record for this chain points to 1C1H. During the relocation process, the loader saves the current contents of the address field, then replaces them with the actual address of the entry to DosOpen. The saved value, if it is not FFFFH, points to the next target that must be adjusted similarly in order to point to the same destination. The special value

FIGURE 2: *Flag Word in OS/2 .EXE Header*



The flag word at offset CH of the header indicates the general characteristics of the program contained in the .EXE file. Many bits are unused in current versions of the operating system, allowing for the incorporation of future enhancements.

TABLE 5: *Relocation Records*

OFFSET	LENGTH	DESCRIPTION
		RELOCATION PREFIX
0H	Byte	Type of relocation target: 2: 16-bit segment value 3: 16-bit segment and 16-bit offset 5: 16-bit offset 11: 16-bit segment and 32-bit offset 13: 32-bit offset
1H	Byte	Destination flag: 0: Within this .EXE file 1: Ordinal in a DLL 2: Name in a DLL (if bit 2 is set, relocation is additive)
2H	Word	Offset of relocation target in this segment
		IF DESTINATION FLAG=0
4H	Byte	Segment number of destination
5H	Byte	Reserved
6H	Word	Destination offset
		IF DESTINATION FLAG=1
4H	Word	Module number of destination
6H	Word	Ordinal of entry point in module
		IF DESTINATION FLAG=2
4H	Word	Module number of destination
6H	Word	Offset of name in imported name table

Each segment carries its own relocation information. The relocation record format depends on the type of external reference: another segment within the same program, a DLL function called by number, or a DLL function called by name.

FFFFH indicates the end of the chain and the end of processing for this relocation record.

How the loader determines the current address of the destination depends on the destination type. When the destination is in the same .EXE file as the target (the flag byte is zero), the destination segment and offset are carried in the relocation record itself. If the target requires segment relocation (byte 0 of the relocation record is 2, 3, or 11), the loader inserts the selector for the destination segment number into the segment field of the target. If the target offset needs relocating (byte 0 is 3 or 5), the loader copies the destination offset from the relocation record into the offset field of the target. If the flag byte indicates additive relocation, the loader adds the values from the relocation record to the target address fields instead of replacing them; in that case, the target cannot be part of a linked list.

If the destination flag is 1, the destination is a function in a DLL, and the function is identified not by its name but by the ordinal number of its entry point in the list of entry points of that DLL. This relocation process is illustrated in figure 3.

The loader uses the module number from the relocation record as an index into the program's module reference table. There it finds an offset into the imported name table. From the latter, it obtains an ASCII string specifying the name of the DLL file containing the destination. If this file is not already in memory, the loader interrupts the current relocation process to load the DLL and perform whatever relocation it requires. This is a recursive process because this DLL may in turn require the loading of other DLLs.

Once the DLL is loaded and mapped into the calling program's LDT, the loader resumes the interrupted relocation process. It scans the entry table of the DLL to find the entry point whose number is specified in the calling program's relocation record. The entry point is identified by a segment number within the DLL and an offset within that segment.

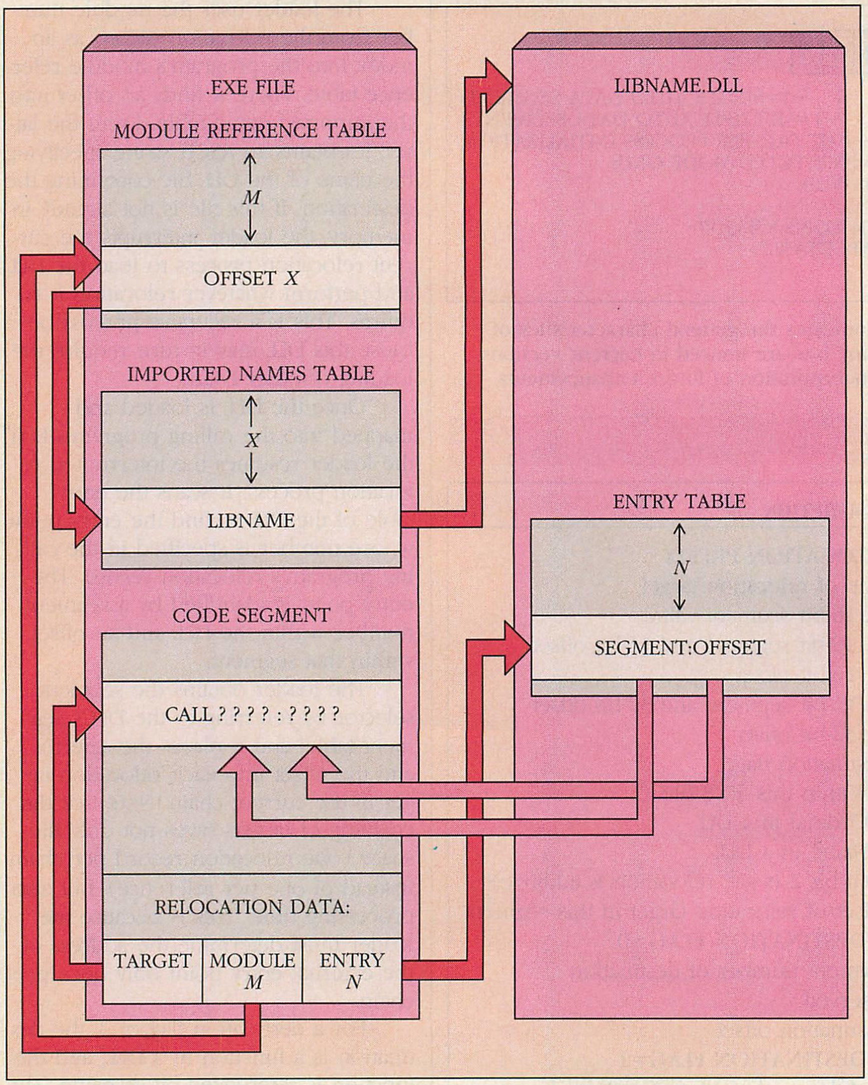
The loader obtains the segment selector by referring to the DLL's segment table, and it places the selector and the offset into each relocation target in the current chain. Note that the chaining of targets saves not only file space (one relocation record per chain instead of one per reference), but also processing time. This is because the loader must determine the address of the external entry point only once per chain.

For a destination flag of 2, the destination is a function in a DLL, and the function is referenced by its name. The loader follows the same procedure as above to find the DLL. Then it uses the name offset from the relocation record as an index into the imported name table of the calling program. In this table it finds an ASCII string specifying the name of the called function. It searches for that name in the resident name table of the DLL; that table provides an ordinal number of the function's entry point. From that point, the process proceeds as above.

Debugging. The Microsoft OS/2 languages support the CodeView debugger, which requires additional descriptive information in the .EXE file. For example, CodeView needs to know all the symbols within the program, even if they are not exported. It also must know the structure of the data areas the program uses.

A bit in the flag word of the segment table record indicates the presence of debugging information for a segment. If present, the information

FIGURE 3: ***Dynamic Linking by Ordinal Position***



One of the major tasks undertaken by the OS/2 loader is locating dynamically linked procedures in external files. In one linking method, the calling program specifies called procedures by their position (ordinal) in the dynamic link library.

follows the relocation data. (The format of this CodeView information is proprietary to Microsoft.)

Imported name table. This table contains the names of DLL modules and the functions within them that the .EXE file calls. The table forms a central repository for all the external names; encoding multiple references to names as offsets into this table saves considerable space over repeating the name string at each reference in a relocation record. The linker normally produces items in this table when it resolves an external reference to an import library such as DOSCALLS.LIB (which contains the import information for the OS/2 API functions). You also can introduce items directly into the table via the IMPORTS statement in the module definition file.

The table begins with a dummy byte containing 0, so that the first name has a nonzero offset. Each table entry consists of a byte containing the name length, followed by the name encoded as an ASCII string. C programmers, take note: the name strings are not terminated by null bytes. A program must use the length byte when manipulating the name. This is also true of the ASCII strings in the other name tables.

The location of the table relative to the start of the OS/2 header is recorded in the word at offset 2AH of the header. Unlike the other tables, however, the imported name table does not have a null byte as a terminator, and the new .EXE header does not give its size.

This is not a problem during normal operation because the items in the imported name table are accessed directly by offsets in relocation records or obtained from the module reference table. However, a program that scans this table must locate its end by using the pointer to the table that follows the imported name table; this is the entry table for the moment, but that is not guaranteed for future versions of OS/2.

Module reference table. This array of 16-bit words forms a cross-reference between module numbers that identify DLLs in relocation records and offsets into the imported name table. The *n*th word in the table contains a value that is an offset to the name of the module that is identified in relocation records as module *n*.

Resident and nonresident name tables. Together, these two tables contain all public names specified to the linker in EXPORT statements. You can specify exported symbols in any .EXE file without incurring an error, but they are meaningful only when you build a DLL file. Both tables have the same format, consisting of variable-length entries.

Each entry begins with a byte that contains the length of the name. Next comes the name encoded as an ASCII string, followed by a 16-bit word that contains the ordinal number of that name's entry point in the entry table. C programmers should be aware that the name string is not terminated by a null byte, but a null byte does follow the last entry in the table. In other words, you have reached the end of the table when the length byte is 0.

The location of the name table (relative to the start of the OS/2 header) is found in the word at offset 26H of the header. The first item in the resident name table is the module name. If the linker does not encounter a NAME statement in the module definition file, it uses the base name of the .EXE file.

For example, if the linker is building a file called PROG.EXE, the default module name would be PROG. Because the module name item is not actually an entry point for the module, its ordinal number is 0. The remaining items, if any, are the symbols that are exported by name rather than ordinal number, plus the symbols exported in both ways.

The nonresident name table differs from the other tables in that its location is given in the header in terms of the offset from the start of the file, not from the OS/2 header. Recording this location in a double word allows for the possibility of a DOS section that exceeds 64KB.

The nonresident name table contains a module description as its first item. If the linker does not encounter a DESCRIPTION statement in the module definition file, it uses the complete .EXE file name. For example, if the linker is told to build a file called D:\MYSTUFF\PROG.EXE, that name becomes the default description. As with the module name, this first item has an ordinal number of 0 because it does not refer to an item in the entry table. The remaining items in the nonresident name table are the exported symbols that are referenced by ordinal number rather than by name.

When OS/2 loads a DLL, it keeps the resident name table in memory so that references to the DLL function names can be resolved quickly. As described above, the table provides a cross-reference between named entry points and their ordinal numbers. Given a name from a calling program, the loader searches this table to find the entry point's ordinal position. The nonresident name table is not kept in memory—these function names are referenced by their ordinal numbers, which require only the entry table.

Entry table. Specifying the entry points of all exported functions, the entry table consists of one or more *bundles*, each of which begins with a two-byte prefix (see table 6). The first byte indicates the number of entry points defined in the bundle; the second byte gives the bundle type. Except for a null bundle, a three- or six-byte record for each entry point in the bundle follows the prefix. Two bytes containing 0 follow the last bundle. Because only DLLs typically contain exported entry points, in most .EXE files this table is empty, consisting of two 0 bytes.

This bundled format saves file space, but it complicates the task of locating the entry table item for an ordinal number. Instead of using the ordinal number as an index into the table, the loader must scan through the bundles, counting items until it reaches the correct one. The entry points in this table are numbered from 1, not 0.

Entry points exported by name are ordered automatically by the linker; the exports by ordinal are specified by the programmer in EXPORT statements in the module definition file. Numbers need not start at 1, nor do they need to be contiguous. Null bundles in the entry table serve as placeholders for the missing numbers. For example, if the lowest ordinal in a module is 12H, the first bundle is null and the count value in its first byte is 11H.

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TABLE 6: *Entry Records*

OFFSET	LENGTH	DESCRIPTION
		BUNDLE PREFIX
0H	Byte	Number of entries in bundle
1H	Byte	Bundle type: 00H: Null bundle, no records FFH: Movable segment records *nn*H: Fixed segment records for segment *nn*
		MOVABLE SEGMENT RECORD (6 bytes)
0H	Byte	Flags: 1=Exported entry 2=Uses shared data segment
1H	2 bytes	Fixed value: CDH 3FH
3H	Byte	Segment number containing entry point
4H	Word	Offset of entry point
		FIXED SEGMENT RECORD (1 byte)
0H	Byte	Flags, as above
1H	Word	Offset of entry point

The entry table lists each entry point of a dynamic link library. Entry points are identified by ordinal number or by position in this table. Bundling the entry points by segment reduces the size of the entry table but requires locating an entry point by scanning the table instead of using the ordinal as an index.

Resource table. The resource table was introduced for Windows, and it also will be used for the OS/2 Presentation Manager. This table specifies the graphic resources the program requires, such as dialog boxes and menus. This table's content and format are not defined for OS/2 1.0. Version 5.01 of the OS/2 linker sets the resource table pointer (offset 24H of the OS/2 header) to the address of the resident name table. However, the word at offset 34H gives the number of resource-table entries; a zero value here indicates that the table is absent.

READING A HEADER

The quickest—but not the easiest—way to examine an OS/2 .EXE file is with a binary editor or debugger (you must rename an .EXE file to examine its header with a debugger). An easier way is to use a program (such as listing 1, SHOWEXE.C) that formats and prints out the headers from both DOS and OS/2 executable files and the various tables from the latter. SHOWEXE.C can be compiled with either the Lattice C or Microsoft C OS/2 compilers; binding it into a family-mode program allows it to run under either DOS or OS/2. Its output goes to the standard output device, so you can redirect it easily to a printer or file. If it is not redirected, the screen display pauses after processing each section of the file.

An example of a practical application that needs to process an .EXE file header is a benchmarking program that examines the segment table and reports the true memory requirement of the program in that .EXE file. Although larger programs usually have larger .EXE files, it is no longer accurate to judge the memory efficiency of different compilers or languages by simply comparing the .EXE sizes that they produce. You could adapt the section of SHOWEXE.C that prints out the segment table for this purpose; similarly, you could extract other parts of interest instead of using the whole program.

The OS/2 segmented executable file format is an extension of the DOS .EXE format, and it has been used in Microsoft Windows for several years. It has evolved to support OS/2 protected mode and DLLs. The new .EXE format also includes several features quite obviously intended for future versions of OS/2, including a resource table for Presentation Manager and embryonic support of the 32-bit capabilities offered by the 80386. Fortunately, as with the DOS version, the OS/2 .EXE format has been designed for easy incorporation of future enhancements.

David A. Schmitt is president of Lattice Inc., a subsidiary of SAS Institute. Schmitt has recently directed the adaptation of the entire Lattice C library to OS/2.

LISTING 1: SHOWEXE.C

```
/*
 * SHOWEXE displays information about the EXE file named on the
 * command line.  It can handle both the DOS and the OS/2 formats.
 * If output is not redirected, it pauses after each section.
 * Written by David A. Schmitt.
 */
#include <stdio.h>
extern far pascal VioScrollUp();
extern far pascal VioWrtCharStr();
extern far pascal VioWrtNAttr();
extern char *malloc();

extern void pause();
extern void cls();
/**
*
* Old executable header, used by DOS
*
*/
struct EXE_DOS
   {
   unsigned short e_magic;    /* magic number 0x5A4D      */
   unsigned short e_cblp;     /* bytes in last page       */
   unsigned short e_cp;     /* 512-byte pages in file  */
   unsigned short e_crlc;     /* number of relocations    */
   unsigned short e_cparhdr;  /* paragraphs in header     */
   unsigned short e_minalloc; /* minimum extra paragraphs  */
   unsigned short e_maxalloc; /* maximum extra paragraphs  */
   unsigned short e_ss;      /* initial SS value       */
   unsigned short e_sp;      /* initial SP value       */
   unsigned short e_csum;     /* checksum               */
   unsigned short e_ip;      /* initial IP value       */
   unsigned short e_cs;      /* initial CS value       */
   unsigned short e_lfarlc;    /* file address of reloc table  */
   unsigned short e_ovno;      /* overlay number        */
   unsigned short e_res1[4];  /* reserved              */
   unsigned short e_oemid;     /* OEM identifier         */
   unsigned short e_oeminfo;  /* OEM information        */
   unsigned short e_res2[10]; /* reserved              */
   unsigned long  e_lfanew;    /* file address of new header    */
   };
/**
*
* Structure of DOS relocation items
*
*/
struct REL
   {
   unsigned short offset;
   unsigned short segment;
   };
/**/
/**
```

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```
 *
 * New executable header, used by OS/2
 *
 */
struct EXE_OS2
   {
   unsigned short ne_magic;   /* magic number 0x454E  */
   unsigned char ne_ver;      /* version number    */
   unsigned char ne_rev;      /* revision number       */
   unsigned short ne_enttab;  /* offset of entry table*/
   unsigned short ne_cbenttab;   /* # of bytes in entry table*/
   long ne_crc;             /* checksum          */
   unsigned short ne_flags;   /* miscellaneous flags      */
   unsigned short ne_autodata;   /* auto data segment number    */
   unsigned short ne_heap;    /* initial heap allocation */
   unsigned short ne_stack;   /* initial stack allocation    */
   unsigned short ne_ip;      /* initial IP offset     */
   unsigned short ne_cs;      /* initial CS segment number*/
   unsigned short ne_sp;      /* initial SP offset     */
   unsigned short ne_ss;      /* initial SS segment number*/
   unsigned short ne_cseg;    /* number of segments        */
   unsigned short ne_cmod;    /* number of module references    */
   unsigned short ne_cbnrestab;  /* size of non-resident names*/
   unsigned short ne_segtab;  /* segment table offset     */
   unsigned short ne_rsrctab; /* resource table offset     */
   unsigned short ne_restab;  /* resident name table offset */
   unsigned short ne_modtab;  /* module reference table offset*/
   unsigned short ne_imptab;  /* import name table offset    */
   unsigned long ne_nrestab;  /* non-resident name tab offset  */
   unsigned short ne_cmovent; /* number of movable entries  */
   unsigned short ne_align;   /* segment alignment shift count*/
   unsigned short ne_cres;    /* number of resource entries */
   char resv[10];           /* reserved        */
   };
/**
 *
 * Definition of bits in ne_flags
 *
 */
#define NENOTP 0x8000      /* not a process        */
#define NEIERR 0x2000      /* errors in image          */
#define NEFLTP 0x0080      /* floating point instructions */
#define NEI386 0x0040      /* 80386 instructions       */
#define NEI286 0x0020      /* 80286 instructions       */
#define NEI086 0x0010      /* 8086 instructions        */
#define NEPROT 0x0008      /* protected mode only      */
#define NEPPLI 0x0004      /* per-process library initialization*/
#define NEINST 0x0002      /* per-instance data        */
#define NESOLO 0x0001      /* solo data            */
/**
 *
 * Structure of segment table entries
 *
 */
struct SEG
   {
   unsigned short ns_sector;  /* starting sector       */
   unsigned short ns_cbseg;   /* segment size (in file)*/
   unsigned short ns_flags;   /* segment flags      */
   unsigned short ns_minalloc;   /* minimum size in bytes*/
   };
/**
*
* Definition of bits in ns_flags
*
*/
#define NSTYPE 0x0007      /* segment type mask, types are...  */
#define NSCODE 0       /*    0 for code segment    */
#define NSDATA 1       /*    1 for data segment    */
#define NSITER 0x0008      /* iterated segment         */
#define NSMOVE 0x0010      /* movable segment          */
#define NSPURE 0x0020      /* pure segment             */
#define NSPRELOAD 0x0040   /* preloaded segment     */
#define NSEXRD 0x0080      /* code segment: execute only*/
                  /* data segment: read only */
#define NSRELOC 0x0100     /* relocation information present   */
#define NSCONFORM 0x0200   /* conforming segment       */
#define NSDPL 0x0c00    /* 80286 DPL bits        */
#define SHIFTDPL 10        /* shift factor for NSDPL  */
#define NSDISCARD 0x1000   /* discardable segment      */
#define NS32BIT 0x2000     /* 32-bit segment         */
#define NSHUGE 0x4000      /* huge memory segment      */
/**/
/**
*
* name      main -- main program
*
* synopsis  main(argc,argv)
*     int argc;       number of arguments
*     char *argv[];       argument pointer array
*
* description:
* This is the main program that displays EXE file information.
*     Upon entry, argc should be 2, and argv[1] should point to
*     the EXE file name, which must include the .EXE extension.
*
*     The program sends its output to stdout, which can be
*     redirected to somewhere other than the system console.
*     Error output is sent to stderr, and when an error occurs
*     the program exits with a completion code of 1.
**/
main(argc,argv)
int argc;
char *argv[];
{
FILE *fp;
unsigned char *p;
int i,j,k;
union
   {
   short w;
   char b[2];
   } word;
struct EXE_DOS oldexe;
struct REL rel;
struct EXE_OS2 newexe;
struct SEG seg;
char b[256];
/*
*
* Check file argument, open file, and read old EXE header
*
*/
if(argc < 2)
   {
   fprintf(stderr,"No EXE file specified\n");
   exit(1);
   }
fp = fopen(argv[1],"rb");
if(fp == NULL)
   {
   fprintf(stderr,"Can't open \"%s\"\n",argv[1]);
   exit(1);
   }
if(fread((char *)(&oldexe),sizeof(struct EXE_DOS),1,fp) != 1)
   {
   fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
   exit(1);
   }
if(oldexe.e_magic != 0x5a4d)
   {
   fprintf(stderr,"\"%s\" is not an EXE file\n",argv[1]);
   exit(1);
   }
/*
*
* Print DOS header information
*
*/
cls();
printf("DOS EXE header information for \"%s\"...\n\n",argv[1]);
printf("%40s: %u\n","Number of bytes in header",oldexe.e_cparhdr*16);
printf("%40s: %u\n","Number of 512-byte pages",oldexe.e_cp);
printf("%40s: %u\n","Number of bytes in last page",oldexe.e_cblp);
printf("%40s: %04XH\n","Checksum",oldexe.e_csum);
printf("%40s: %04XH\n","Minimum number of extra paragraphs",
       oldexe.e_minalloc);
printf("%40s: %04XH\n","Maximum number of extra paragraphs",
       oldexe.e_maxalloc);
printf("%40s: %04X:%04X\n","Starting address",oldexe.e_cs,
       oldexe.e_ip);
printf("%40s: %04X:%04X\n","Stack address",oldexe.e_ss,
```

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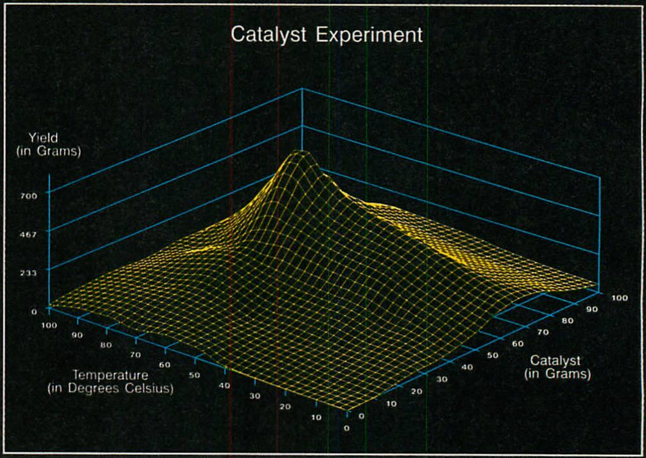

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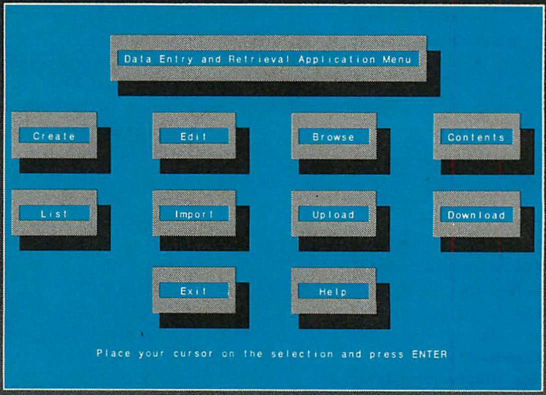

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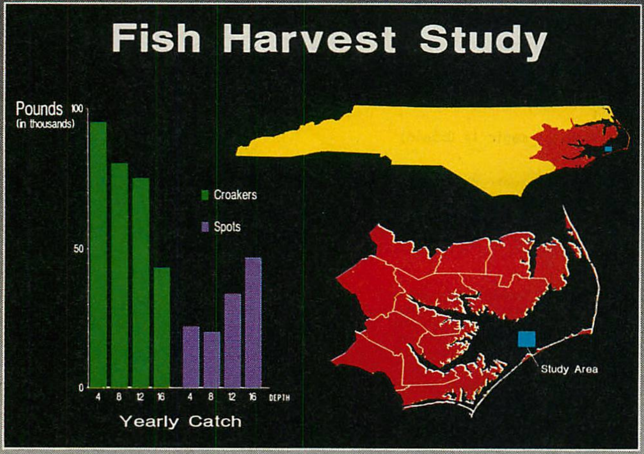

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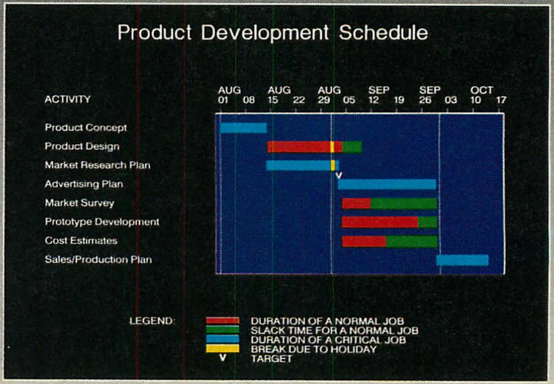

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```
        oldexe.e_sp);
printf("%40s: %u\n","Overlay number",oldexe.e_ovno);
printf("%40s: %04XH\n","OEM identifier",oldexe.e_oemid);
printf("%40s: %04XH\n","OEM information",oldexe.e_oeminfo);
printf("%40s: %u\n","Number of relocations",oldexe.e_crlc);
/*
 *
 * Print DOS relocation table
 *
 */
if(oldexe.e_crlc)
   {
   pause(fp);
   printf("\n\nRelocation table at file offset %04XH...\n",
      oldexe.e_lfarlc);
   if(fseek(fp,(long)oldexe.e_lfarlc,0))
      {
      fprintf(stderr,"Can't seek to %04XH in \"%s\"\n",
         oldexe.e_lfarlc,argv[1]);
      exit(1);
      }
   for(i = 1; i <= oldexe.e_crlc; i++)
      {
      if(fread((char *)(&rel),sizeof(struct REL),1,fp) != 1)
         {
         fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
         exit(1);
         }
      printf("%04X:%04X  ",rel.segment,rel.offset);
      if((i % 6) == 0) printf("\n");
      }
   }
/*
 *
 * Check if OS/2 executable, and terminate if not.
 * Otherwise, read in the OS/2 header.
 *
 */
if(oldexe.e_lfanew == 0) exit(0);
pause();
```

```
printf("\n\nOS/2 EXE header information at %04XH...\n\n",
      oldexe.e_lfanew);
if(fseek(fp,(long)oldexe.e_lfanew,0))
   {
   fprintf(stderr,"Can't seek to %04XH in \"%s\"\n",
     oldexe.e_lfanew,argv[1]);
   exit(1);
   }
if(fread((char *)(&newexe),sizeof(struct EXE_OS2),1,fp) != 1)
   {
   fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
   exit(1);
   }
if(newexe.ne_magic != 0x454e)
   {
   fprintf(stderr,"\"%s\" is not an OS/2 EXE file\n",argv[1]);
   exit(1);
   }
/*
 *
 * Print basic information from new EXE header
 *
 */
printf("%40s: %08lXH\n","Checksum",newexe.ne_crc);
printf("%40s: %u\n","Version number",newexe.ne_ver);
printf("%40s: %u\n","Revision number",newexe.ne_rev);
printf("%40s: %u\n","Number of segments",newexe.ne_cseg);
printf("%40s: %04X:%04X\n","Starting address",
       newexe.ne_cs,newexe.ne_ip);
printf("%40s: %04X:%04X\n","Stack address",newexe.ne_ss,newexe.ne_sp);
printf("%40s: %u\n","Automatic data segment number",
       newexe.ne_autodata);
printf("%40s: %04XH\n","Initial heap allocation in auto data",
       newexe.ne_heap);
printf("%40s: %04XH\n","Initial stack allocation in auto data",
       newexe.ne_stack);
printf("%40s: %04XH\n","Flags",newexe.ne_flags);
printf("%40s? %s\n","Program or library",
   (newexe.ne_flags & NENOTP) ? "LIBRARY" : "PROGRAM");
printf("%40s? %s\n","Errors in image",
```

```
    (newexe.ne_flags & NEIERR) ? "YES" : "NO");
printf("%40s? %s\n","Floating point instructions",
    (newexe.ne_flags & NEFLTP) ? "YES" : "NO");
printf("%40s? %s\n","80386 instructions",
    (newexe.ne_flags & NEI386) ? "YES" : "NO");
printf("%40s? %s\n","80286 instructions",
    (newexe.ne_flags & NEI286) ? "YES" : "NO");
printf("%40s? %s\n","8086 instructions",
    (newexe.ne_flags & NEI086) ? "YES" : "NO");
printf("%40s? %s\n","Protected mode only",
    (newexe.ne_flags & NEPROT) ? "YES" : "NO");
printf("%40s? %s\n","Per-process initialization",
    (newexe.ne_flags & NEPPLI) ? "YES" : "NO");
printf("%40s? %s\n","Per-instance data",
    (newexe.ne_flags & NEINST) ? "YES" : "NO");
printf("%40s? %s\n","Solo data",
    (newexe.ne_flags & NESOLO) ? "YES" : "NO");
pause();
/*
 *
 * Print segment table
 *
 */
printf("\n\nSegment table at %08lXH (%08lXH + %04XH)...\n\n",
      (long)(oldexe.e_lfanew+newexe.ne_segtab),
      oldexe.e_lfanew,newexe.ne_segtab);
printf("     FILE  FILE        MEMORY\n");
printf("SEG  ADDR  SIZE  FLAGS   SIZE\n\n");
if(fseek(fp,(long)(oldexe.e_lfanew + newexe.ne_segtab),0))
  {
  fprintf(stderr,"Can't seek to %08lXH in \"%s\"\n",
      (long)(oldexe.e_lfanew+newexe.ne_segtab),argv[1]);
  exit(1);
  }
for(i = 1; i <= newexe.ne_cseg; i++)
  {
  if(fread((char *)(&seg),sizeof(struct SEG),1,fp) != 1)
    {
    fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
    exit(1);
    }
  printf("%3d  %04X  %04X  %04X    %04X  %s\n",i,
     seg.ns_sector,seg.ns_cbseg,seg.ns_flags,seg.ns_minalloc,
     (seg.ns_flags & NSTYPE) ? "Data" : "Code");
  }
pause();
/*
 *
 * Print imported name table
 *
 */
if(newexe.ne_imptab)
  {
  printf("\n\n");
  printf("Imported Name Table at %08lXH (%08lXH + %04XH)...\n\n",
        (long)(oldexe.e_lfanew+newexe.ne_imptab),
        oldexe.e_lfanew,newexe.ne_imptab);
  if(fseek(fp,(long)(oldexe.e_lfanew + newexe.ne_imptab + 1),0))
    {
    fprintf(stderr,"Can't seek to %08lXH in \"%s\"\n",
       (long)(oldexe.e_lfanew+newexe.ne_imptab + 1),argv[1]);
    exit(1);
    }
  printf("INDEX  NAME\n");
  printf("-----  ----\n");
  for(i = newexe.ne_imptab+1; i < newexe.ne_enttab; i += j+1)
    {
    j = fgetc(fp);
    if(j == EOF)
      {
      fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
      exit(1);
      }
    if(j == 0) break;
    if(fread(b,j,1,fp) != 1)
      {
      fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
      exit(1);
      }
    b[j] = '\0';
    printf(" %04x  %s\n",(i-newexe.ne_imptab),b);
    }
  pause();
  }
/*
 *
 * Print Module Reference Table
 *
 */
if(newexe.ne_cmod)
  {
  printf("\n\n");
  printf("Module Reference Table at %08lXH (%08lXH + %04XH)...\n\n",
       (long)(oldexe.e_lfanew+newexe.ne_modtab),
       oldexe.e_lfanew,newexe.ne_modtab);
  if(fseek(fp,(long)(oldexe.e_lfanew + newexe.ne_modtab),0))
    {
    fprintf(stderr,"Can't seek to %08lXH in \"%s\"\n",
       (long)(oldexe.e_lfanew+newexe.ne_modtab),argv[1]);
    exit(1);
    }
  printf("MODULE  INDEX\n");
  printf("------  -----\n");
  for(i = 1; i <= newexe.ne_cmod; i++)
    {
    if(fread((char *)(&j),2,1,fp) != 1)
      {
      fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
      exit(1);
      }
    printf(" %04X   %04X\n",i,j);
    }
  pause();
  }
/*
 *
 * Print Resident Name Table
 *
 */
if(newexe.ne_restab)
  {
```

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```
printf("\n\n");
printf("Resident Name Table at %08lXH (%08lXH + %04XH)...\n\n",
       (long)(oldexe.e_lfanew+newexe.ne_restab),
       oldexe.e_lfanew,newexe.ne_restab);
if(fseek(fp,(long)(oldexe.e_lfanew + newexe.ne_restab),0))
   {
   fprintf(stderr,"Can't seek to %08lXH in \"%s\"\n",
      (long)(oldexe.e_lfanew+newexe.ne_restab),argv[1]);
      exit(1);
   }
   printf("ORDINAL  NAME\n");
   printf("-------  ----\n");
   while(i = fgetc(fp))
      {
      if((i == EOF) || (fread(b,i,1,fp) != 1))
         {
         fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
         exit(1);
         }
      b[i] = '\0';
      if(fread((char *)(&j),2,1,fp) != 1)
         {
         fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
         exit(1);
         }
      printf("   %04X  %s\n",j,b);
      }
   pause();
   }
/*
*
* Print Non-resident Name Table
*
*/
if(newexe.ne_nrestab)
   {
   printf("\n\nNon-resident Name Table at %08lXH...\n\n",
      newexe.ne_nrestab);
   if(fseek(fp,newexe.ne_nrestab,0))
      {
      fprintf(stderr,"Can't seek to %08lXH in \"%s\"\n",
         newexe.ne_nrestab,argv[1]);
      exit(1);
      }
   printf("ORDINAL  NAME\n");
   printf("-------  ----\n");
   while(i = fgetc(fp))
      {
      if((i == EOF) || (fread(b,i,1,fp) != 1))
         {
         fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
         exit(1);
         }
      b[i] = '\0';
      if(fread((char *)(&j),2,1,fp) != 1)
         {
         fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
         exit(1);
         }
      printf("   %04X  %s\n",j,b);
      }
   pause();
   }
/*
*
* Print entry table
*
*/
if(newexe.ne_cbenttab)
   {
   printf("\n\nEntry table at %08lXH (%08lXH + %04XH)...\n\n",
      (long)(oldexe.e_lfanew+newexe.ne_enttab),
      oldexe.e_lfanew,newexe.ne_enttab);
   if(fseek(fp,(long)(oldexe.e_lfanew + newexe.ne_enttab),0))
      {
      fprintf(stderr,"Can't seek to %08lXH in \"%s\"\n",
            (long)(oldexe.e_lfanew+newexe.ne_enttab),argv[1]);
      exit(1);
      }
   p = malloc(newexe.ne_cbenttab);
   if(p == NULL)
      {
      fprintf(stderr,"Out of memory\n");
      exit(1);
      }
   if(fread(p,newexe.ne_cbenttab,1,fp) != 1)
      {
      fprintf(stderr,"Can't read \"%s\"\n",argv[1]);
      exit(1);
      }
   printf("SEG  OFFSET  FLAGS\n");
   printf("---  ------  -----\n");
   for(i = 0; i < newexe.ne_cbenttab; )
      {
      j = p[i++];
      k = p[i++];
      if(k) while(j-- > 0)
         {
         if(k != 255)
            {
            word.b[0] = p[i+1];
            word.b[1] = p[i+2];
            printf("%3d  %04X    %02X\n",k,word.w,p[i]);
            i += 3;
            }
         else
            {
            word.b[0] = p[i+4];
            word.b[1] = p[i+5];
            printf("%3d  %04X    %02X\n",p[i+3],word.w,p[i]);
            i += 6;
            }
         }
      }
   }
}
/**/
/**
*
* name      pause
*
* synopsis  pause();
*
* description  This function checks if the standard output file
*      is the system console.  If so, it displays a pause message
*      and then waits until the user presses a key.
*
**/
void pause()
{
char reverse = 0x70;
static char prompt[] = "Press any key to continue";

if(isatty(fileno(stdout)))
   {
   VioWrtNAttr((char far *)(&reverse),80,24,0,0);
   VioWrtCharStr((char far *)prompt,sizeof(prompt)-1,24,0,0);
   getch();
   cls();
   }
}
/**
*
* name      cls -- clear the screen
*
* synopsis  cls();
*
* description  This function clears the screen by calling the
*      VioScrollUp function in a special way.  However,
*      it has not be generalized to work with display
*      modes using more than 25 lines of 80 characters each.
*
**/
void cls()
{
short fill = 0x0720;

VioScrollUp(0,0,24,79,-1,(short far *)(&fill),0);
}
```

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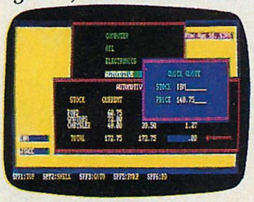

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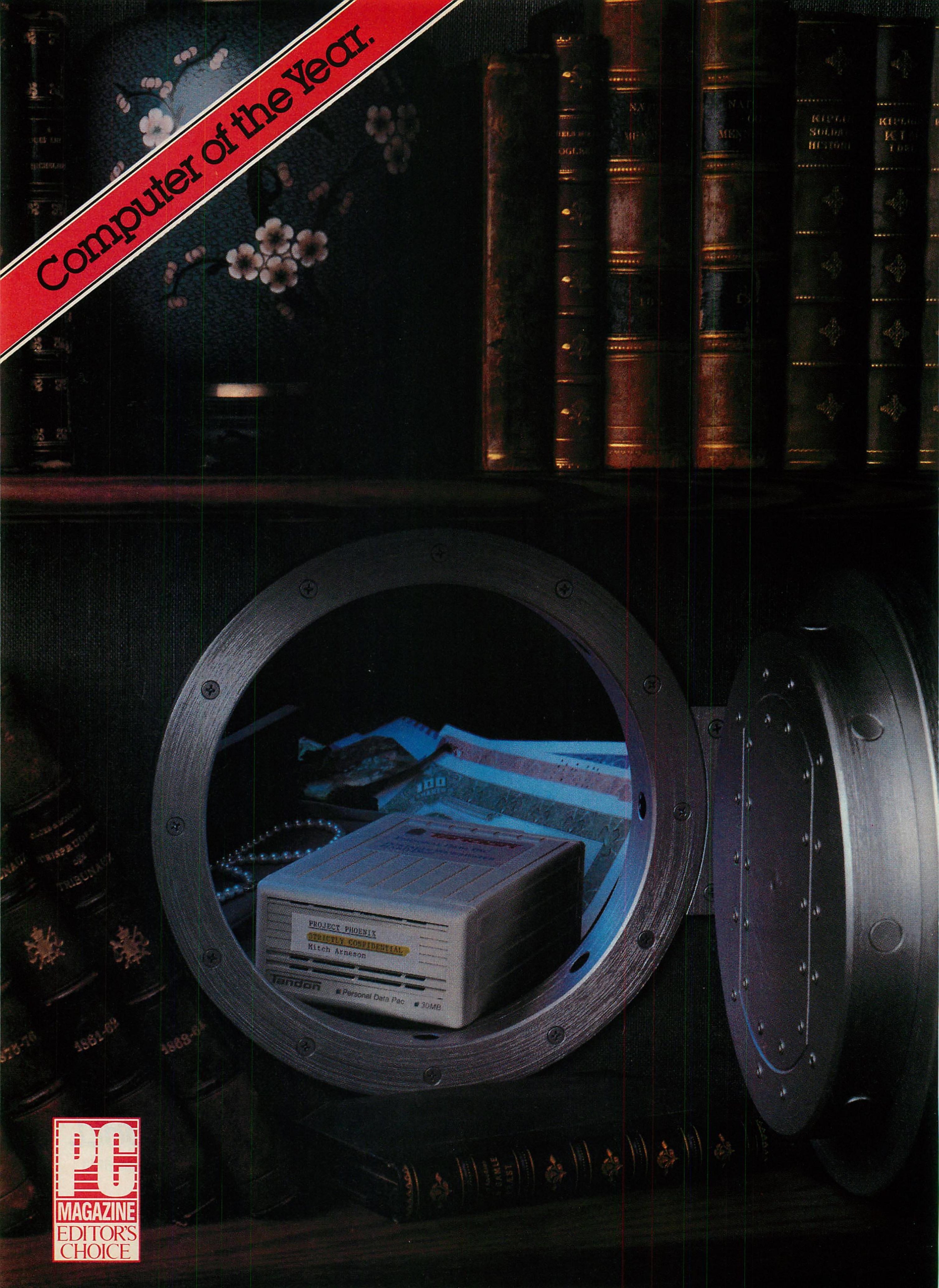
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The Tandon Ad-PAC

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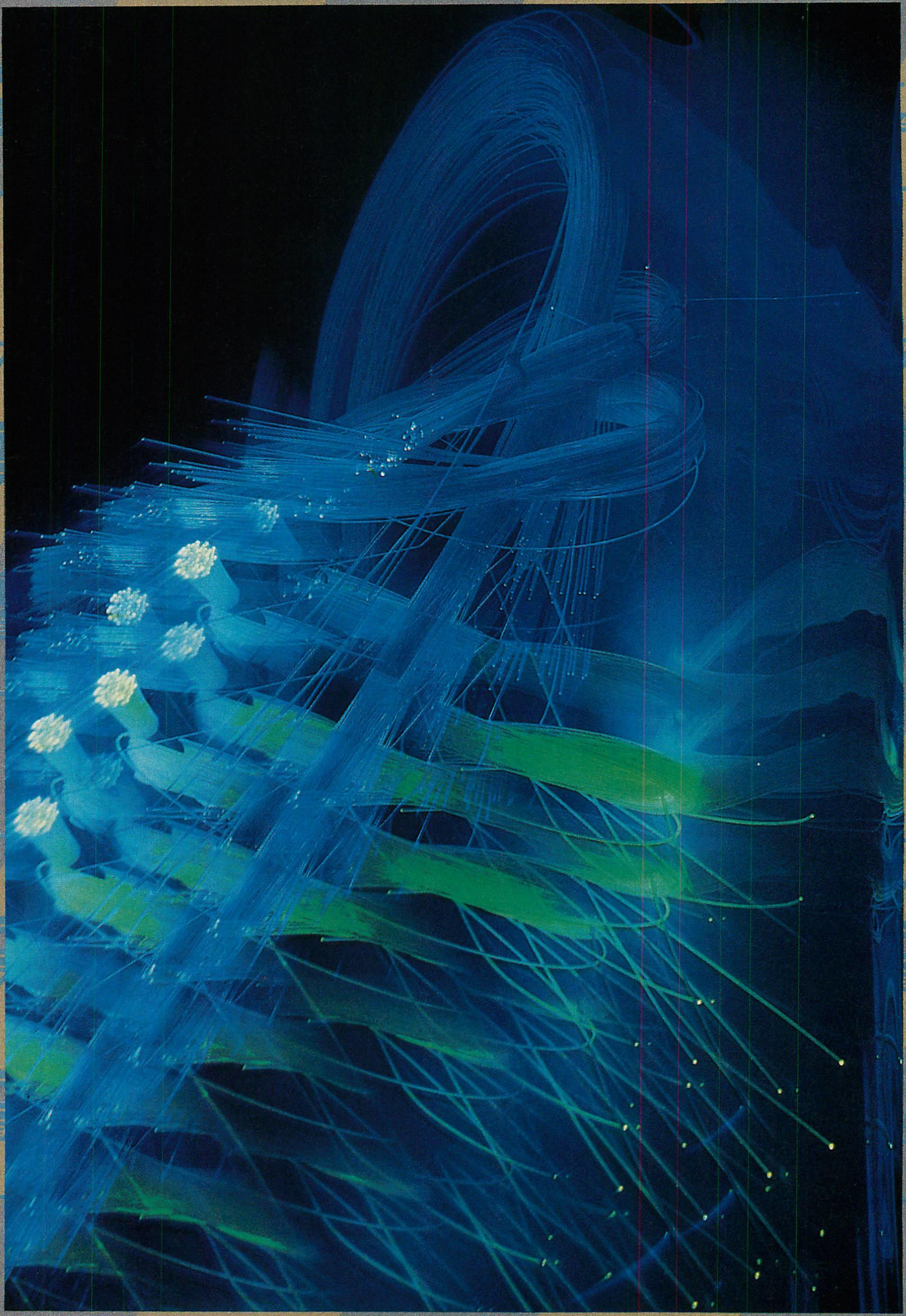

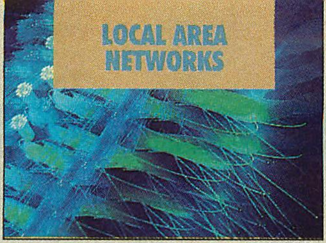

Bright Lights, Fast LANs

Fiber optics, capable of massive bandwidth, high speed, and long distance, may be the future for network connections. An evolving ANSI standard and commercial implementations signal the onset of this new technology.

ALAN C. WU

In the raging, unsettled, unstandardized LAN industry, the impending proliferation of yet another technology may not be received with much favor—unless it's fiber optics. The allure is obvious: the potential for incredibly high bandwidths, combining voice, data, and even video communications on a single, thin, strong, electrically nonconductive medium.

Until recently, LAN administrators had good grounds for not widely embracing fiber optics. The components were expensive; trained technicians were few; the installed base of LANs was built principally on copper-based coaxial cable and twisted-pair wire; the technology was unfamiliar; and no clear standard for fiber-optic communications was established.

Such hindrances, though, are fading rapidly. Optical-fiber LANs are available today in standard topologies—Ethernet, Arcnet, token-ring. Costs for existing topologies are within reasonable range of more traditional ones, and, although scarce, trained technicians can be found. Most importantly, a standard for this technology—called the Fiber Distributed Data Interface (FDDI)—has been proposed by ANSI committee X.3T9.5, which includes representatives from IBM, AT&T, DEC, NASA, and the U.S. Navy. This standard carries with it the promise of wide acceptance for optical fiber in the LAN marketplace.

FDDI is a descendant of the IEEE 802.5 token-ring protocol; it is the only standard developed for a high-performance, general-purpose, fiber-optic LAN. It specifies a 100-megabits per second (Mbps), fiber-optic, token-ring architecture that supports 1,000 nodes with 2 kilometers (km) between adjacent nodes and a 200-km ring circumference. The FDDI specification sets no lower limits on the number of nodes or the distances between them.

Some companies that market fiber-optic LANs have said they will upgrade their products to FDDI compliance once the standard is fully adopted; one firm, Fibronics International, already markets an implementation of the all-but-complete standard. Fiber optics can be implemented in a network under several topologies, although each topology carries advantages and disadvantages.

With its high data rate, FDDI can be implemented for both back-end networks—connecting host mainframes with storage devices—and front-end networks—connecting PCs and peripherals. It supports high-speed engineering workstations and graphics terminals. LAN designers also can apply FDDI in backbone networks to support low-speed IEEE 802 LANs. Its deterministic timed token protocol guarantees channel access. FDDI also accommodates traffic from distributed private branch exchanges (PBXs). Figure 1 shows a sample FDDI configuration.

Fiber optics has long been used in telecommunications networks to supplant coaxial cable as the medium for

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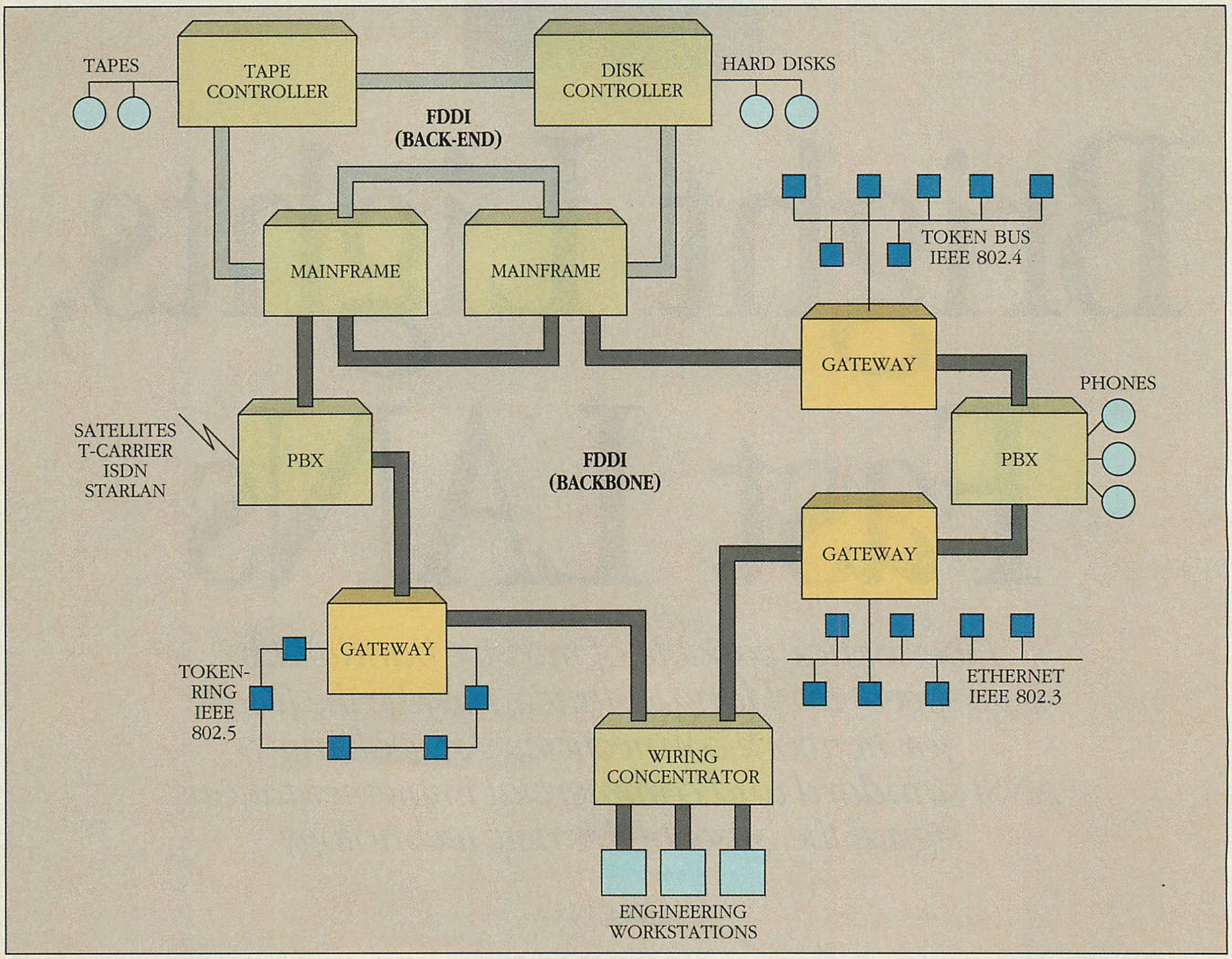
FIGURE 1: ***FDDI Back-end and Backbone Configuration***



FDDI links provide high-speed back-end communications to peripherals, such as disk drives on hosts, as well as front-end backbones to a variety of communications services. Here, several different kinds of LANs are connected via the FDDI backbone.

high-bandwidth, long-distance transmission links. Its low *attenuation* (signal loss) enables optical fiber to transmit high-speed data over tens of kilometers without repeaters, which makes it an excellent medium for data communications over wide areas and between buildings. Optical fiber transmits information using light, so it is immune to electromagnetic interference, impulse noise, and crosstalk; in addition, the fibers do not radiate energy, so they cause little interference with other equipment. Thus, optical fiber is ideal for high-noise areas, such as factories.

Coaxial cable and twisted-pair wire are, of course, the traditional transmission media for LANs. Twisted-pair is popular for its relatively low cost, small size, and ease of installation (see "A New Twist for Ethernet," John Kolman, September 1988, p. 86). Its major drawbacks are limited distance and a susceptibility to electrical interference. Compared with twisted-pair, coaxial cable is more expensive and is larger and more difficult to install, but it supports many more devices over significantly longer distances.

The surge in engineering workstations and high-performance PCs that need to move millions of bytes of data quickly is beginning to tax the limits of copper wire. Back-end networks require higher capacities and speed to connect mainframes to storage devices such as hard disks and optical disks. Backbone networks, which transfer data among mainframes, LANs, or distributed PBXs—and which require greater capacity to support internetworking traffic as well as to carry realtime voice information—are exhibiting similar growing pains.

In addition, the rapid expansion of corporate networks and factory automation systems spurs new demands for large, integrated communications networks that carry data, voice, and video simultaneously. As companies assess their maturing performance requirements and the cost of installing LANs, the benefits of optical fiber in terms of bandwidth, distance, and speed recommend it for present and future needs. Only optical fiber delivers the bandwidth/distance performance required by more and more users.

LIGHT-HEARTED

Although still the new kid on the network block, optical fiber soon will be one of the first choices when LAN designers and administrators start choosing sides. Its many compelling properties, including high bandwidth, low signal attenuation, excellent security, electromagnetic isolation, and small cable size, make it a heavy hitter.

Bandwidth. The potential bandwidth and, hence, transmission rate, of a cabling medium increases with its fre-

quency. Optical carrier frequency is approximately 10^{14} to 10^{15} Hz, which is 10 million times greater than coaxial cable. The potential bandwidth of optical fiber is tremendous; however, today's fiber transmits at rates far below its theoretical capacity. Signal dispersion and attenuation (discussed below) are the limiting factors.

Dispersion. Figure 2 shows three constructs of optical fiber. A *step-index multimode* fiber consists of a cylindrical glass core, about 50 to 100 micrometers (μm) in diameter, with a constant index of refraction, surrounded by cladding material with a lower refractive index. A light pulse enters the core and travels down the fiber by means of total internal reflection. The optical fiber acts as a waveguide for light. Differing path lengths of transmission, due to multiple angles of incidence of the rays into the fiber, result in multimodal light in the fiber.

Each mode of light has a different length path to travel. A ray traveling straight along the axis of the fiber reaches its destination before a ray that bounces down with many reflections. The bouncing leads to a broadening of the initial light pulse, called *modal dispersion*, which, in turn, causes interference between successive data bits. This interface limits the effective bandwidth and, thus, slows the transmission rate of the fiber.

Cores with a *graded-refractive-index* profile minimize modal dispersion. Here, the light pulse is refocused continuously as it travels within the fiber. Rays speed up as they pass into the lower-refractive-index glass, so that all rays arrive at the destination at approximately the same time. This reduces pulse dispersion by three orders of magnitude relative to step-index fiber, substantially increasing effective bandwidth.

Material dispersion, which results when the refractive index of glass varies with respect to the transmission wavelength, also causes pulse spreading. Different wavelengths of light propagate at different speeds in the fiber, producing a smeared pulse. Material dispersion increases as the spectral width of the light source increases. If a transmitted pulse is truly monochromatic, the variation of its refractive index would have no effect.

The number of modes, N, supported in step-index fiber is

$$N = 2(\pi a/\lambda)^2 (n_1^2 - n_2^2)$$

where a is the core radius, λ is the wavelength of the light, n_1 is the core index of refraction, and n_2 is the cladding index of refraction.

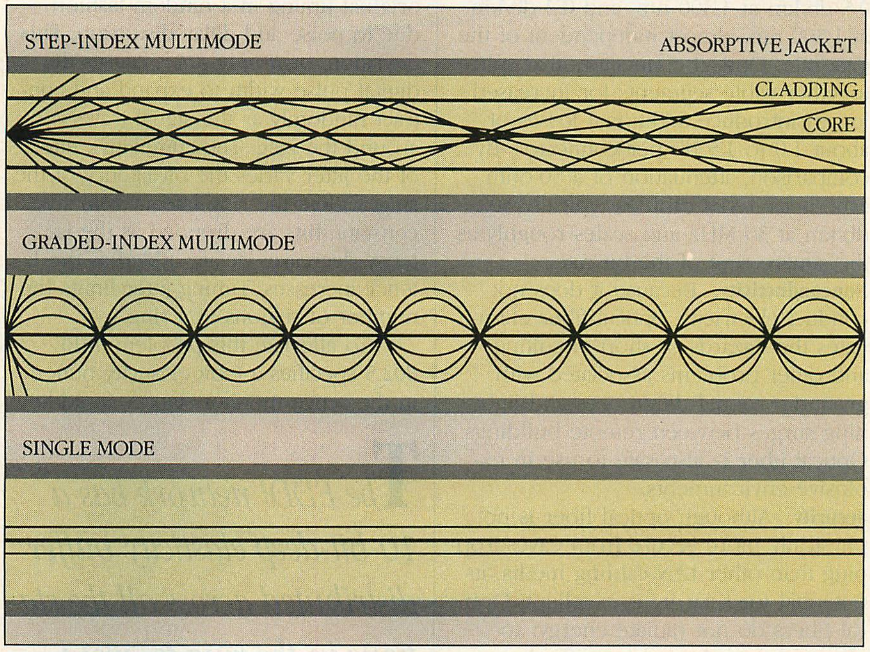
If a, n_1, and n_2 are selected such that $N = 1$, the result is a fiber that supports a *single mode* of propagation, in which modal dispersion cannot occur. Only material dispersion can cause signal dispersion of a single-mode fiber, which typically has a core diameter of 8 μm or less. Even this effect is minimal if the light source has a narrow spectral width—as with a laser. The bottom line is that single-mode fiber has the highest potential bandwidth and, thus, can support higher data rates over longer distances than can multimode fiber. The catch is that single-mode fiber *must* use a laser as its light source, significantly increasing complexity, expense, and risk of equipment failure. (FDDI does not require single-mode fiber.)

Because optical-fiber bandwidth varies according to the length of the transmission medium, bandwidth is always given for a specific distance, usually 1 km. The typical bandwidth of optical fiber is as high as 200 MHz/km for step-index multimode fiber, between 200 MHz/km and 3 GHz/km for graded-index multimode fiber, and from 3 GHz/km to 50 GHz/km for single-mode fiber. This tremendous capacity far exceeds that of coaxial cable or twisted-pair wire; moreover, it enables a single fiber to carry voice, data, and video simultaneously via *wavelength division multiplexing* (analogous to frequency division multiplexing, or FDM, on a broadband network).

Attenuation. Signal loss, or attenuation, in optical fiber is due primarily to absorption, material scattering, and waveguide scattering. Impurities and inconsistencies in the fiber material cause absorption and material scattering, respectively; geometric irregularities at the interface between the fiber-optic core and its cladding cause waveguide scattering. Unlike coaxial cable, optical-fiber attenuation is not a function of signal frequency, but of the fiber material and the wavelength of the light source.

Either a light-emitting diode (LED) or a laser can be the light source for an optical fiber. Light with wavelengths of about 850, 1,300, and 1,500 nanometers (nm) propagates best in silica glass optical fiber and suffers less attenuation. In addition, attenuation is generally lower at higher wavelengths—the reason for the greater data rates over longer distances.

FIGURE 2: ***Three Grades of Optical Fiber***



Light rays are depicted moving through the three types of optical-fiber cable. In step-index multimode fiber, light travels by constant refraction, causing much modal dispersion of the initial pulse of light. This limits the effective bandwidth and, thus, its transmission rate. Graded-index multimode fiber constantly refocuses the rays, thus minimizing modal dispersion. Single-mode fiber has the highest potential bandwidth, but requires a light source with a narrow spectral width—such as a laser. Single-mode achieves data rates in the gigabytes-per-second range, but its cost is too high for uses other than long-distance telecommunications.

Typical fiber attenuation is 2 decibels per kilometer (db/km) at 850 nm, 0.5 db/km at 1,300 nm, and 0.2 db/km at 1,500 nm, almost independent of the data rate. Optical connectors that splice together cable segments for increased length introduce additional losses of about 1.0 to 1.5 db per connector. By comparison, attenuation of a 50-ohm Ethernet coaxial cable is typically 30 db/km at 30 MHz and scales roughly as the square root of the bit rate.

Nonconductivity. Because it does not conduct electricity, optical fiber eliminates the hazards of short circuiting and other problems associated with ground-potential differences and lightning surges between remote buildings. Optical fiber is also safe to use in explosive environments.

Security. Although optical fiber is not physically more secure from eavesdropping than other LAN cabling media, its potential for security is excellent. Optical fibers do not radiate energy, so electronic monitoring is ineffective without a physical connection, and it is difficult to tap the fiber without interrupting communications. Thus, for *complete* security, you must control access to the cable and monitor the signal continually.

Size. Optical fiber is easily made into long lengths with uniform dimensions. Unit lengths of several kilometers are common, with much longer lengths possible. A 125-μm-diameter fiber that is 1 km long takes up only 12 cubic centimeters and weighs 28 grams. It is also quite flexible and strong, so it is much easier to transport, install, and pull through wire-runs and ducts than coaxial cable. For cramped conduits in buildings and underground along public rights-of-way, optical fiber's size and flexibility are invaluable.

FDDI LIGHTS THE WAY

ANSI has been approving the proposed FDDI standard in piecemeal fashion, but it is close to complete adoption. Proponents of fiber-optic technology see FDDI as a standard for high-performance LANs that is necessary to interconnecting the increasingly sophisticated computers of the future. The FDDI standard embraces all levels of LAN operation.

Clocking. FDDI's predecessor, IEEE 802.5, uses self-clocking differential Manchester encoding (DME). (See "The Token-Ring Solution," J. Scott Haugdahl, January 1987, p. 50 for more information.) As each station receives data, the timing information is recovered from the incoming bit stream, which, in turn, is used for transmitting data to the next station. The clocking deviates from the original timing in a random fashion due to noise and delay distortion. This deviation, or *timing jitter*, causes the digital pulse width to expand and contract randomly as the signal travels around the ring. The cumulative effect of the jitter varies the bit latency of the ring. Unless the ring latency remains constant, bits are dropped as the latency decreases or are added as the latency increases. Timing jitter limits the number of stations in a ring.

To alleviate this problem, IEEE 802.5 specifies a 6-bit elasticity buffer in the active monitor station, in addition to requiring a phase-locked loop in each repeater. Bits are clocked into the buffer at the rate recovered from the incoming stream, but they are clocked out at the station's crystal master clock rate. The elasticity buffer expands and contracts to avoid dropping or adding bits.

The FDDI network has a 10-bit-deep elasticity buffer distributed across all the stations in the ring to avoid dropping or inserting bits.

The buffer of the centralized monitor would be prohibitively large to accommodate FDDI's high data rate. To eliminate the cumulative timing-jitter effect in FDDI, each station recovers the clocking from the incoming bit stream. The outgoing stream is clocked by the local fixed-frequency oscillator. Unless some compensation is included, the accuracy of the oscillator (required to be stable to 0.005 percent), which allows the incoming frequency to be slower or faster than the outgoing frequency, results in an excess or deficiency of bits.

The FDDI network has a 10-bit-deep elasticity buffer distributed across all the stations in the ring to avoid dropping or inserting bits. This distributed system is more robust than the 802.5 6-bit buffer and minimizes jitter. The reclocking at each station eliminates constraints on the number of repeaters on the ring.

The transmitter clock also is stable to 0.005 percent. With an elasticity buffer of 10 bits, stations can transmit frames as long as 4,500 octets without exceeding the buffer's limits.

Data encoding. The DME scheme is only 50-percent efficient: it is adequate for the 4-Mbps data rate of the IEEE 802.5 token-ring LAN, but inefficient for FDDI. Were FDDI to use DME to reach the specified 100 Mbps, it would require a signaling rate of 200 megabaud (Mbaud)—which could be achieved only with expensive laser diodes and avalanche photo diodes (so called for the *avalanche breakdown*, in which voltage becomes virtually independent of current).

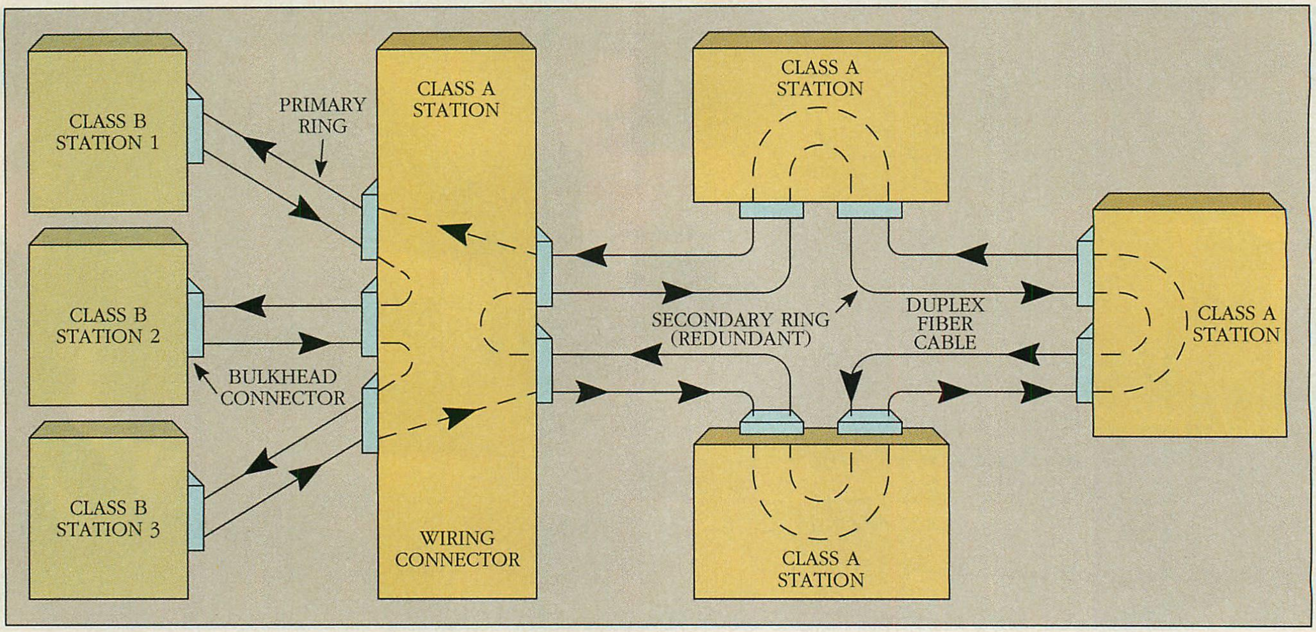
To overcome DME's data-rate inefficiency, FDDI specifies the 4-bit/5-bit (4b/5b) encoding scheme, in which encoding is done 4 bits at a time to create a five-cell symbol on the medium. Each set of 4 bits is, in effect, encoded as 5 bits. The efficiency is raised to 80 percent, so that 100 Mbps is achieved with 125 Mbaud—well within the realm of relatively inexpensive LEDs and PIN diodes (shorthand for a P-segment to N-segment with a connecting, or In-between, module). The lower signal rate also lowers the cost of the circuitry associated with the network.

To provide reliable data reception and bit synchronization, the 4b/5b binary stream is encoded further into a nonreturn-to-zero-inverted (NRZI) format before transmission to the fiber.

Access. Similar to IEEE 802.5, the FDDI medium access is based on a token that circulates when all stations are idle. A station must seize a passing token before it can transmit. An IEEE 802.5 station seizes the token by flipping the T-bit (token-bit) from 0 to 1 in the access control field of the token frame. However, FDDI's high data rate renders this impractical. Under FDDI, the station seizes the token by absorbing the token transmission upon recognition. When the token is received completely, the station begins transmitting frames. The station continues to transmit until it has no more data to transmit or until the token-holding timer (THT) expires.

The station originating a frame is responsible for removing it from the ring when it completes a round-trip. When the transmission is terminated, the transmitting station generates a new token. However, if the ring bit length is greater than that of the frame, a new token is issued by the originating station before the leading edge of the current frame returns to its transmitter to be purged. This feature allows two tokens to be on the network at one

FIGURE 3: ***FDDI Dual-ring Configuration***



FDDI combines two independent, counter-rotating rings. Each runs at 100 Mbps—the effective throughput is 200 Mbps when they operate simultaneously. If the primary ring fails, the secondary ring provides a backup to sustain 100 Mbps. Class A stations connect to both rings, continuing on a single ring if one ring fails; the less-critical class B stations connect to one ring.

time (an IEEE 802.5 node must wait for the transmitted frame to return before inserting a new token). FDDI's scheme is more efficient in large ring configurations because it allows the network to transmit multiple frames from different stations at the same time.

Transmission medium. FDDI specifies graded-index multimode silica glass fibers with core/cladding diameters of 50/125, 62.5/125, or 85/125 μm. Single-mode fiber is not required to meet FDDI performance goals. This is significant because although single-mode and multimode fibers cost about the same, the transmitters, receivers, switches, and connectors for single-mode are significantly more expensive than multimode equivalents.

In addition, multimode fiber can use either a laser or an LED light source. Although lasers generate more power and have a much narrower spectral width than LEDs, they are far more complex and, consequently, more expensive. Lasers also have a shorter life span than LEDs. FDDI specifications are based on the more economical component—the less expensive and longer-lived LEDs.

Fiber-optic light sources generally operate at one of three wavelength windows—850, 1,300, or 1,500 nm. Only LEDs at 850 nm and 1,300 nm are available commercially today; however, because LEDs have comparatively wide spectra, chromatic dispersion is one of the primary effects that limits link bandwidth. FDDI, therefore, specifies the 1,300-nm wavelength so that, at the FDDI rate of 125 Mbaud, chromatic dispersion would limit short wavelength operation to distances of only a few hundred meters. The 1,300-nm wavelength has a lower attenuation and causes minimal chromatic dispersion, permitting much longer distances.

FDDI specifies a minimum peak output of -16 dbm (a measure of power relative to 1 milliwatt) from optical transmitters, which LED-based light sources can achieve, and a minimum receiver input of -27 dbm for a bit error rate of one in $2.5 * 10^{10}$ bits transmitted. PIN diodes can handle this; the more expensive avalanche photo diodes are not necessary. The total link power budget (the amount of signal loss allowed in transmission between sending and receiving units), therefore, is 11 db. A 2-km length of high-quality fiber loses less than 5 db, leaving approximately 6 db for other signal attenuators, including splices, connectors, and switches. The typical FDDI connector loss is less than 1 db.

Rings. As figure 3 illustrates, FDDI combines two independent, counter-rotating, primary and secondary rings. Each ring runs at 100 Mbps; the effective throughput is 200 Mbps when the two operate simultaneously. If the primary ring fails, the secondary ring provides a backup to sustain 100 Mbps.

In a 1,000-node configuration, the average distance between adjacent nodes must be 200 meters to keep the ring circumference within the 200-km limit. Nodes can be separated by as much as 2 km as long as the average separation does not exceed 200 meters. No lower limit is imposed on node separation distance.

The FDDI limits maintain ring latency—that is, the time it takes a signal to travel around the ring—within a few milliseconds, depending on the outcome of the bidding process. Minimum ring latency is critical for many real-time network applications.

Station types. FDDI defines two station types: class A stations, which are either mainframes or wiring concentrators, connect to both primary and secondary rings; the less-critical class B stations connect to only one of the rings, thus reducing station hardware costs. If a cable breaks, class A stations reconfigure the dual ring into a single ring, keeping all nodes in operation. If the network sustains two faults, it can split itself into two smaller rings that operate separately.

Class A stations repeat information on both rings, so file servers and other stations that provide critical network services should be class A connections. Workstations or microcomputers are usually class B stations because they can change location in an evolving business environment. Wiring con-

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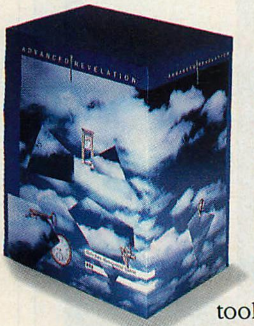

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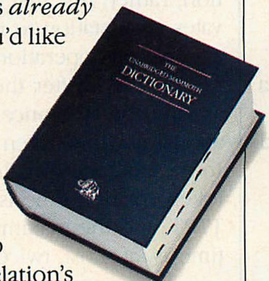

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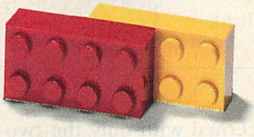

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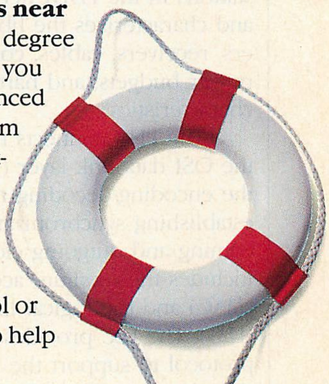

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centrators can mitigate the effects of such relocations on the network and verify that such stations are operating properly when reconnected.

Architecture. Figure 4 shows the relationship between the FDDI architecture and both the IEEE 802.5 structure and the Open System Interconnection (OSI) layered protocol. IEEE 802.5 specifies a 4-Mbps, token-ring LAN using shielded, twisted-pair wire. However, the high data rate of FDDI, which is 25 times better than that of IEEE 802.5, creates many differences between the two, specifically in the physical layer. Protocols that work well with low-speed networks do not necessarily meet the requirements when data rates are scaled up by an order of magnitude.

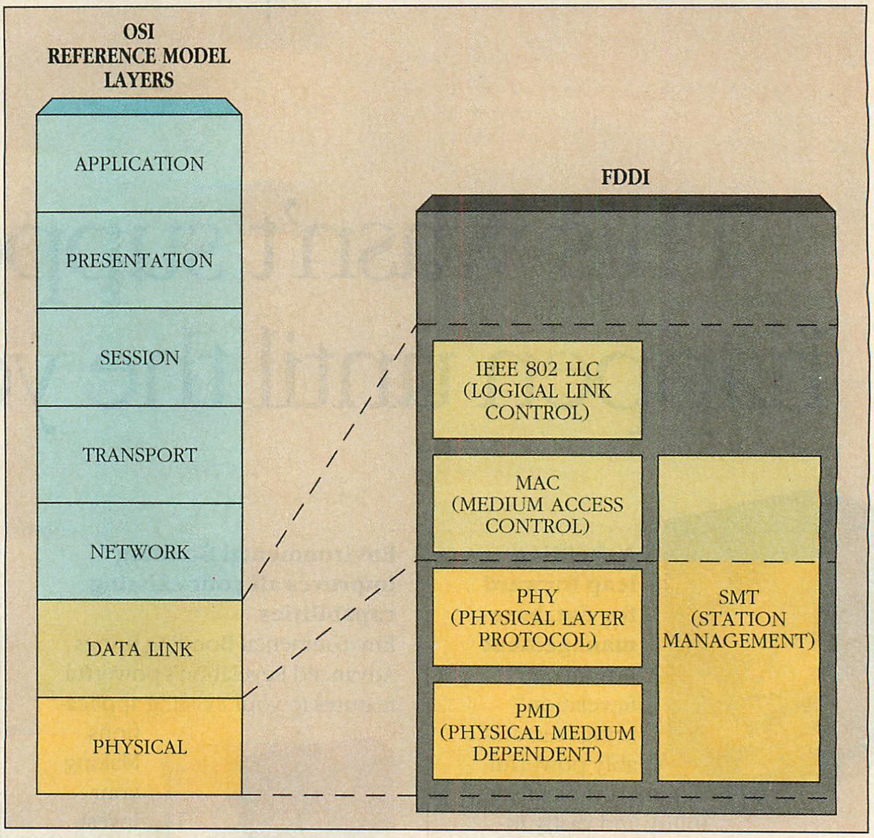
The OSI physical layer (PL) is divided into two FDDI sublayers, the physical medium dependent (PMD) and the physical layer protocol (PHY). The PMD provides the digital baseband point-to-point communication between stations in the FDDI network. It defines and characterizes the fiber-optic drivers, receivers, cables, connectors, power budgets, and hardware-related characteristics.

The PHY connects the PMD and the OSI data link layer (DLL), supplying the encoding/decoding mechanism and establishing synchronization for the incoming and outgoing clocks. The DLL includes the medium access control (MAC) and the logical link control (LLC). The LLC provides a common protocol to support the required services between MAC and the OSI network layer (NL). The FDDI uses the LLC developed by IEEE 802.2.

The MAC provides fair and deterministic medium access, address recognition, and generation, as well as verification of frame check sequences. It defines the timed-token protocol, which ensures that a station can transmit a minimum amount of data on the ring within a predictable amount of time. MAC's primary role is to deliver frames, including insertion, repetition, and removal. The FDDI MAC interface is compatible with IEEE 802.2 LLC.

Station management (SMT) is part of network management, and it resides in each station. SMT provides services such as configuration-management control, fault isolation and recovery, and scheduling procedures to ensure the station's proper operation as a member of the ring. Figure 5 shows FDDI's frame and token formats. The frame size is limited to 4,500 bytes, sufficient for most applications, to accommodate the distributed clocking scheme.

FIGURE 4: ***FDDI's Relationship to the OSI Model***



FDDI is concerned with only the two lowest levels of the OSI model. The OSI physical layer is divided into two FDDI sublayers, the physical medium dependent (PMD) and the physical layer protocol (PHY). The OSI data link layer includes the medium access control (MAC) and the logical link control (LLC).

Capacity. FDDI controls usage of the network capacity through the timed token rotation (TTR) scheme. Within each station, the MAC transmitter controls ring scheduling with a token rotation timer (TRT), which measures the time elapsed since a token was last received. During initialization, FDDI allows each station to bid for the value of target token rotation time (TTRT) via a continuous stream of claim frames, each of which contains the station's bid in a data field.

Each claiming station inspects the TTRT value of an incoming claim frame, relaying it if the TTRT value is lower than its own. Otherwise, the station replaces the incoming claim frame with its own frame, which contains its bid. The station that requests the shortest TTRT wins. If two or more stations request the same TTRT value, the station with the longest and highest address wins.

Bidding is complete when a station receives its own claim frame, which contains the lowest bidding of the TTRT, after it has made a round-trip on the ring. Each station copies the value of the new TTRT, to allocate channel capacity for all stations. The winning station then can send a token to its downstream neighbor.

In its first cycle on the ring, the token cannot be captured by any station; rather, this first appearance activates each station to move from initialization to its operational state and to reset its TRT. After the token passes around the ring once, the ring is operational and the token can be captured. In the absence of failures, the average token rotation time is, at most, the TTRT, and the maximum token rotation time is, at most, twice the TTRT.

To support a mixture of intermittent and stream traffic, FDDI defines two types of traffic, synchronous and asynchronous. Synchronous traffic has delivery-time constraints; for example, delays in voice and video transmissions can cause serious disruptions in signals. The time constraints of asynchronous traffic are not so stringent.

Synchronous transmission times are preallocated to those stations that support synchronous traffic. A station can transmit synchronous data for the

preallocated time whenever a token is captured. Preallocation ensures that the TTRT is not exceeded, even if every station transmits the maximum synchronous data. Stations that do not support synchronous traffic can transmit only asynchronous traffic. Asynchronous transmissions are permitted only when all of the pending synchronous requests have been serviced and the THT has not expired.

The timed token scheme is based on the token rotation time having a linear relationship to the load on the ring. If the token comes back later than the TTRT, the station assumes a heavy network-transmission load, in which case it can transmit only synchronous frames. When the token comes back sooner than the TTRT, the station assumes a relatively light load. It first transmits synchronous frames for the preallocated time, then (or if no synchronous frames were ready to transmit), the token-holding timer begins running. The station then can transmit asynchronous frames as long as the TRT is less than the TTRT.

This protocol guarantees that, in a normal ring, an average synchronous response time does not exceed the TTRT, and the maximum synchronous response time never exceeds twice the TTRT. Any excess capacity is available for asynchronous traffic.

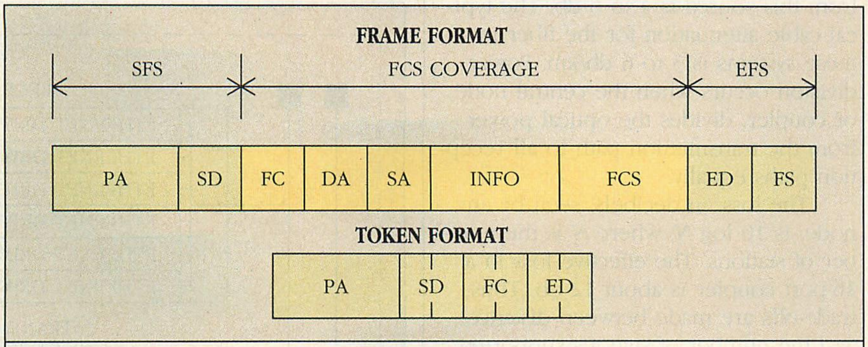
FIBER FORMATIONS

Each of the three basic LAN topologies—ring, star, and bus—can be implemented in optical fiber, under either a passive or an active arrangement. Specific characteristics such as bandwidth, attenuation, power budget, connectability, cost, and access control are important in determining a suitable fiber-optic LAN topology. Among the determinants in choosing a topology for any LAN installation are application requirements, reliability, expandability, and performance.

Fundamental differences between copper media and optical fiber—mainly the former's electrical conductivity and fiber's higher bandwidth potential—render topologies that are suitable for twisted-pair wire or coaxial cable inappropriate for optical fiber. Although FDDI specifies an active ring in this first fiber-optic standard specification, no one configuration is a better overall choice than the others.

Passive star. In a fiber-optic, passive-star LAN, two fibers (one to transmit and one to receive) connect each station to a central unpowered coupler; a single optical transmitter-receiver pair

FIGURE 5: ***FDDI Frame- and Token-format Blocks***



SYMBOL	DESCRIPTION
SFS = Start of frame sequence	Consists of the PA and SD fields of the frame, which together ensure the timing and validity of all tokens and frames.
PA = Preamble	Establishes and maintains clock synchronization. Consists of 16 or more idle symbols (64 bits) transmitted by the frame originator.
SD = Start delimiter	Indicates the start of the frame. The start delimiter consists of two delimiter symbols (JK) that are always distinguishable from data. No frame or token is considered valid unless it starts with this explicit sequence.
FC = Frame control	Defines the types of the frame and associated control functions. Distinguishes between synchronous and asynchronous frames, MAC and LLC frames, length of the address field (16 or 48 bits), and restricted or unrestricted tokens.
DA = Destination address	Identifies the station(s) for which the frame is intended. Addresses can be either 16 or 48 bits long.
SA = Source address	Identifies the station originating the frame. Addresses are the same length as the destination address in a given frame.
FCS = Frame check sequence	Detects erroneous data bits within the frame via a 32-bit cyclic redundancy check.
EFS = End of frame sequence	Consists of ED and FS fields, which ensure a clear close to each frame.
ED = Ending delimiter	Contains nondata symbols to indicate the end of the frame. The delimiter is eight bits long for a token (two consecutive T symbols) and four bits long (a single T symbol) for all other frames.
FS = Frame status	Contains a minimum of three control-indicator symbols that indicate whether the addressed station has recognized its address, the frame has been copied, or any station contains an error in the frame.

Frame-format blocks are assigned to carry data around the network ring, while token-format blocks cycle around the network looking for requester stations.

is required for each station. When a station transmits, the optical signal passes to the central node where it is divided among all the output fibers and is distributed to all of the stations on the network.

Although physically a star, the interconnection acts like a bus: a transmission from one station is received by all. To avoid a collision, which occurs if two stations transmit simultaneously, this configuration uses the carrier sense multiple access with collision detection (CSMA/CD) protocol to control channel access between stations.

Commercially available passive-star LANs, such as those from Codenoll Technology, support several dozen stations at a recommended radial distance of 800 meters. Limitations on the number of stations and the distances between them are imposed by the amount of network attenuation. Such a LAN tolerates a 25- to 28-db optical loss between the transmitter and the receiver; this attenuation is introduced by connectors, fiber impurities, and optical power division.

A typical passive-star network has zero to four connectors in a path from

transmitter to receiver, each with a loss of about 1.0 to 1.5 db; thus, attenuation from this source is 4 to 6 db. The typical cable attenuation for the fiber in these systems is 3 to 6 db/km. Power division occurs when the central node, or coupler, divides the optical power from the transmission path to all reception paths equally.

The loss, in decibels, seen by any node, is 10 log *N*, where *N* is the number of stations. The effective loss in a 16-port coupler is about 12 db. Thus, trade-offs are made between distance and the number of stations supported. For example, a high-performance LED injecting −5 dbm optical power into a passive-star optical fiber requires receivers with a sensitivity of −30 dbm to support 13 stations spanning 500 meters. The number of stations could increase for the same diameter, if more sensitive (and more expensive) receivers are used.

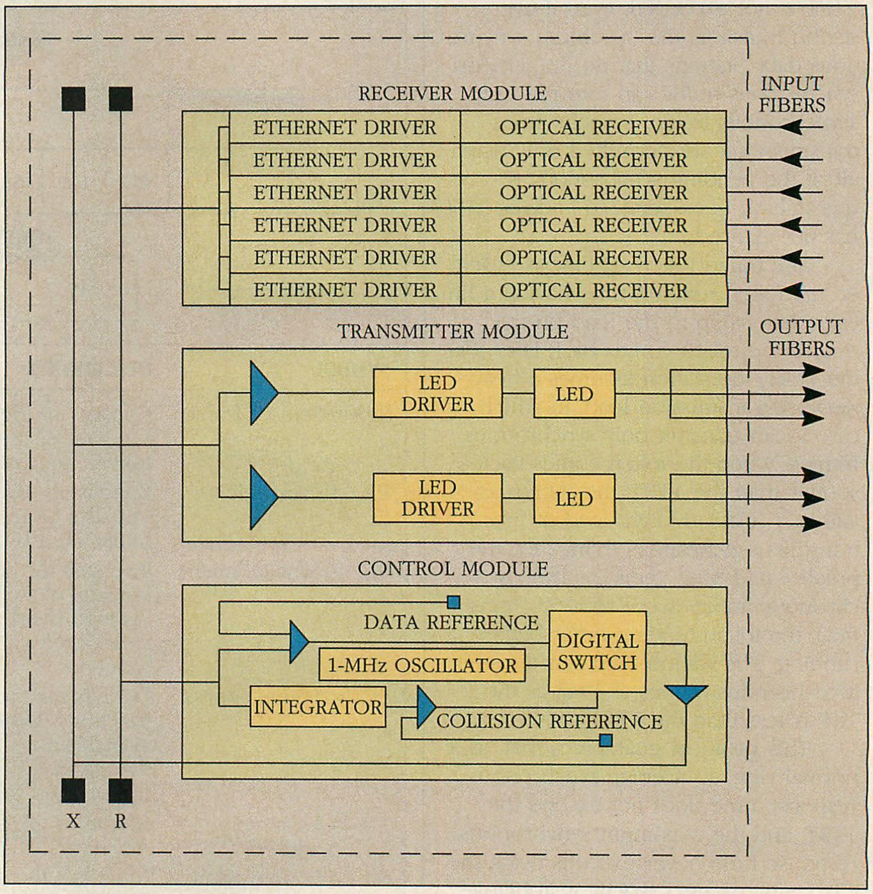
Precisely because the passive star acts like a bus, the fiber-optic transceiver must quickly and reliably detect the presence of more than one signal, or data packet, to avert a collision. This is difficult because packets from other stations could arrive simultaneously and can have considerable variations in optical signal power: a strong packet coming from a station near the star could mask a second, weaker signal coming from a station at maximum distance from the star, when both arrive at the same instant. Collision-detection schemes that attempt to detect differences in received powers or violations of DME are not reliable.

Although this suggests that passive stars are best suited to smaller installations, they can be cascaded off of active-star couplers to build large systems, using available products (from Codenoll Technology, for example). Because they are unpowered, passive-star couplers (which cost about $1,000) are less likely to be a point of failure in a network.

Active star. To circumvent the problems of optical-power dynamic range and reliable collision detection, the central node, or coupler, can be *active*: the powered coupler regenerates the signal before distributing it to the other stations. Thus, an active-star topology supports more stations over a greater distance than a passive star.

Fibernet II, an early design of the Xerox Palo Alto Research Center (and never distributed commercially), is an active-star fiber-optic LAN. Fibernet II supports 100 devices at a radius of 2.5 km. Plug-compatible with Ethernet at

FIGURE 6: *An Active-star Repeater*



The active-star repeater for Ethernet typically uses a copper-based back-plane X bus (to transmit) and R bus (to receive) between input, output, and the control module. X and R handle traffic as optical signals are received, processed as electrical transmissions, and output again as optical pulses via light-emitting diodes.

the transceiver cable interface, Fibernet II functions as either a segment in a large coaxial Ethernet or as a standalone network. Bidirectional transfer of 10-Mbps, DME-encoded data occurs between the active star and the Fibernet transceivers over duplex optical fiber; the transceivers are connected to the station with standard Ethernet cables or connectors.

Figure 6 is a block diagram of an active-star repeater in which three modules are connected through two back-plane, 50-ohm buses called R (for receive) and X (for transmit). The receiver module detects a transmitting station's optical signal on the inbound optical fiber, electrically regenerates its amplitude, and transmits it onto bus R, which is, in fact, a miniature Ethernet. The control module receives the signal and retransmits it through the digital switch onto bus X. Finally, the transmitter module, with its LED transmitters, picks up the signal from bus X and retransmits it optically to all stations via the outbound fibers.

Collision detection, performed in the control module, is accomplished by monitoring the average signal level on the R bus. By converting the optical signal to an electrical one, the design avoids the difficult problem of detecting a collision of optical signals. If two or more stations transmit simultaneously, the collision is detected and the digital switch is set so that a 1.0-MHz collision signal is transmitted to all transceivers.

Fibernet II uses LED sources and PIN photo-diode receivers. The minimum peak power injected into a fiber is 100 microwatts (μw), and the receiver has a sensitivity exceeding −28 dbm. With a 6-db minimum-link margin, 6-db/km attenuation, and four 1.0-db-loss connectors, optical-link power budget calculations indicate that Fibernet II can support a network with stations separated by as much as 2.5 km. This distance is within the 51.2-microseconds (μs) propagation delay budget allowed for a fully configured Ethernet. For a single repeater-to-repeater run,

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distances of 4 km are possible using the Fibernet II design.

In a star topology, a broken fiber does not bring down the entire network. An active-star LAN further boasts high communications reliability, capacity for a large number of stations, equal access for all stations, easy network reconfiguration and maintenance, and cost-effectiveness. It has one significant drawback, however: a power loss on an active-star coupler disables the entire network.

Because Ethernet is based on the limits of copper media, optical fiber's low attenuation and wide bandwidth are not fully realized in Ethernet-compatible fiber-optic LANs. Ethernet-compatible fiber-optic products are available from a number of commercial vendors, including Artel Communications, Codenoll Technology, BICC Data Networks, Chipcom, FiberCom, and SynOptics Communications.

Passive bus. Light is unidirectional; thus, it does not accommodate the bidirectional data transfer that a bus network requires. To overcome this obstacle, a LAN can have two passive optical couplers for each station. Each coupler consists of a transmitter-receiver pair, so that signals are inserted into and extracted from the unidirectional optical fiber. Each of the transmitter-receiver pairs requires a cable with two fibers. The coupler can extract a portion of the optical energy from one fiber for reception and inject optical energy directly into the other fiber for transmission.

Bus configurations also deal with collision detection via CSMA/CD. An idle station knows a collision has occurred by the presence of data on both of its receivers; data on either of its receivers would indicate a collision to a transmitting station.

These accommodations notwithstanding, a passive-bus configuration has several serious drawbacks. The purely optical couplers, which do not involve light-to-electrical conversions, experience significant energy loss, and low-loss optical couplers are not yet available commercially. Each coupler undergoes an approximate 1-db excess insertion loss, which further increases path attenuation.

Another liability of the passive bus is substantial variation in the optical signal level that a station receives. Each station receives the maximum power when an adjacent station transmits; it receives the minimum power in a transmission from a station at the opposite end of the *N*-station bus. The difference between the maximum and minimum signal power depends on the total loss caused by fiber attenuation, connectors, and coupler excess. In a small network (with 10 stations, for example), the receiver dynamic range is greater than 25 db even without the link margin and fiber attenuation loss. As the number of stations increases, the dynamic-range requirement of the receivers increases dramatically, necessitating highly sensitive and high-dynamic-range optical receivers.

Active bus. In an active bus—a far more practical approach than a passive bus—active couplers reestablish the power in the optical signals. This configuration does not restrict the number of stations it supports with respect to optical power. The active bus also eliminates the optical dynamic-range difficulty—it can use LED sources and PIN receivers because it requires a receiver sensitivity of only −30 dbm and an optical dynamic range of 20 db. In addition, collision detection is a straightforward operation: the simultaneous transmission and reception of data is interpreted as a collision.

ANSI X.3T9.5 specifies an active-ring topology in its first standards for a high-speed, wide-bandwidth, fiber-optic network.

Drawbacks to the active bus are similar to those for the passive bus, but not as severe. Bidirectional data transfer requires twice the fiber and twice the transmitters and receivers. Also, the more complex active repeating components run the risk of lower reliability than their passive counterparts.

The active bus also suffers from *edge jitter* (deterioration) in the bit stream as it traverses each coupler. To ensure that each station maintains synchronism with an incoming bit stream, the edge jitter at the station input must be less than (approximately) ±18 ns. Independent of the number of active nodes, each coupler must reestablish the timing of each received packet before sending it on to the next coupler. However, this causes a delay over and above the steady-state propagation delay between the receive and transmit fibers, which renders the CSMA/CD protocol ineffective. The longer the delay, the longer the frame length of a collision fragment for a fixed-length network, which adversely impacts the maximum distance permitted between two stations.

Commercial fiber-optic Arcnet implementations are a specialized subgroup of the active bus; they are compatible with existing coaxial installations. While no speed increase can be realized, greater distances—up to 3.5 km—can be achieved in addition to other fiber-optic advantages.

Passive ring. A ring configuration is particularly suitable for optical-fiber transmission because data transfer is unidirectional. With this configuration, only single, not duplex, optical fibers are required between couplers.

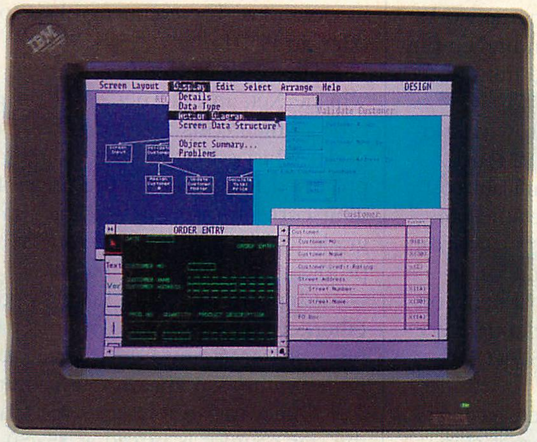
However, the negative aspects of the passive ring heavily outweigh its advantages for most applications. Although node failure need not bring down an entire network, a fiber break certainly will. Further, because signals are not regenerated in the passive ring, this topology suffers from the same optical power budget and cost problems as the passive-bus fiber-optic LAN. The number of nodes supported is likewise limited. The passive-ring topology also has a distinct problem in that once a signal is injected into the fiber, it circulates until completely attenuated, which introduces echoes onto the ring.

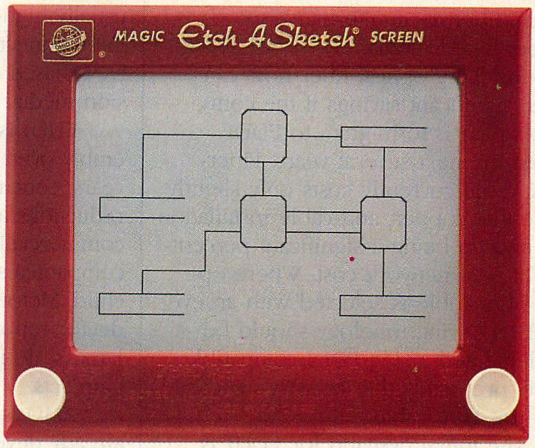
Active ring. An active ring supports a large number of stations over a great distance because regeneration occurs at each node. However, an active ring exhibits the same coupler-delay and circuit-complexity problems as the active-bus fiber-optic LAN. Ring latency, as well as the application response-time requirements and the protocol used to control access to the network, determine the maximum number of stations on the ring.

The active ring is attractive for several reasons: its structural simplicity; the high-performance, medium-access algorithms that have been developed for it; and the sizable network it accommodates. An active-ring fiber-optic LAN holds the greatest growth potential in terms of speed and carrying capacity. ANSI X.3T9.5 specifies the active-ring topology in its first standards for a high-speed, wide-bandwidth, fiber-optic LAN.

LIGHT IN THE FAST LANE

FDDI's most immediate impact is to focus attention on the capabilities of optical fiber. Companies planning to implement high-speed LANs in the





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short term should certainly consider optical fiber as an alternative to copper-based media.

Installing optical fiber now can mean significant savings if the company's plan is to migrate to FDDI within the next several years. Fiber-optic cable currently costs only slightly more that copper, and cable installation can end up being a significant percentage of total network cost. Where optical-fiber cable is selected with an eye to FDDI, a ring topology should be implemented, using FDDI-compatible cable, preferably the industry-standard 62.5-μm core cable.

The initial demand for FDDI is expected to be in backbone networks, but the demand is expected to increase dramatically when the costs of FDDI are reduced so that companies can afford to use it in front-end networks for workstations and microcomputers. Initial FDDI networks will cost about $20,000 or more per node (including cable, couplers, cards, and other costs) but should drop to the $8,000 vicinity as demand and the benefits of mass production reduce per-unit overhead and costs, perhaps by mid-1989. FDDI will not be a widely implemented LAN topology until inexpensive PC boards are available.

Today, more than 50 companies are working on FDDI—Fibronics International has already thrown its hat into the ring. Its system originally cost $70,000 to $100,000 per node—such high price tags have limited FDDI-comparable fiber-optic networks principally to military installations, where high speed and superior security are essential. Such implementations are usually high-speed backbone networks interconnecting Ethernet and token-ring LANs based on lower-speed transmission media.

FDDI is expected to grow considerably over the next three to four years, concurrent with significant cost reductions as FDDI chip sets become commercially available. Semiconductor companies such as AMD, Intel, Fairchild, Motorola, and National Semiconductor reportedly are developing very large scale integration (VLSI) FDDI chip sets.

AMD is the clear leader, having already developed its Supernet chip set, which consists of five chips that perform all necessary FDDI functions for each network node. Supernet is in beta test at numerous sites; the chip set is expected to cost about $625 in quantity, with an adapter card priced at about $5,000.

Full commercial implementations of FDDI are expected by late 1989. This is critical for high-performance workstation manufacturers such as Sun and Apollo, for whom increased transmission speeds are essential to their next generation of workstations.

Several companies that currently market fiber-optic networks are expected to upgrade to FDDI within the next year or two. Among these are Proteon, FiberCom, and Chipcom.

Proteon's ProNET-80 was perhaps the first commercially available fiber-optic LAN to operate at speeds of up to 80 Mbps. Based on the same star-ring architecture as the ProNET-10 system, this LAN relies on a 62.5-μm optical fiber and connects as many as 240 workstations. The company plans to offer an FDDI upgrade.

FiberCom currently offers WhisperNet, an Ethernet on fiber-optic cable, which costs $895 to $2,500 per node. WhisperNet purchasers are promised full credit for the price of their current transceivers if they upgrade to FiberCom's FDDI-compatible products, anticipated in mid-1989.

Chipcom's ORnet is a fiber-optic Ethernet that supports a 10-Mbps data rate and can connect more than 1,000 nodes within 2.5 km without repeaters. The ORnet transceiver costs $545, and the star coupler is priced at $5,450. Chipcom is expected to migrate ORnet to FDDI once protocols are completely defined and chip sets are commercially available.

The FDDI standard supports high-speed, high-capacity applications that cannot be supported by LANs using other transmission media and older IEEE protocols. FDDI is the first standard that is based on the unique characteristics of optical fiber.

As fiber-optic network components, such as connectors and laser diodes, become more reliable, demand will continue to increase and prices will continue to drop. These events will encourage many more applications to exploit the unique talents of optical fiber.

Alan Wu is a staff engineer with Honeywell Bull Inc. in Billerica, Massachusetts, where his responsibilities include performance measurement, analysis, and evaluation of networks and data communications software.

Expert System On-call

Shells that developers embed in conventional software—such as Neuron Data's Nexpert Object—are the next step in the progression of expert-system applications.

TOM ARCIDIACONO

Expert systems have long been considered the most immediately practical application within the academically inclined field of artificial intelligence (AI). To make these systems even more attractive, vendors introduced expert-system shells, which reduce the time and cost of development and open up AI systems to a wide range of non-AI specialists. The latest approach that holds the most promise for the foreseeable future is expert-system shells that developers integrate into conventional software.

One product that has been particularly successful is Neuron Data's Nexpert Object, a powerful hybrid rule- and frame-based shell originally developed for the Macintosh but available for the PC since November 1986. A developer can embed Nexpert beneath the covers of conventional software to provide an internal decision-making capability that otherwise would be impossible. Conclusions reached by Nexpert's inference engine can trigger external programs and, conversely, external programs can initiate the Nexpert inferencing process.

Delivered as a set of C functions, Nexpert can be integrated into programs written in a variety of languages, such as Ada, FORTRAN, C, and Pascal, and the system can directly access popular relational databases (Oracle Corporation's ORACLE, Relational Technology Inc.'s INGRES, and Sybase Inc.'s SYBASE) via Structured Query Language (SQL) queries, Ashton-Tate's dBASE III PLUS, Lotus 1-2-3, and, in the near future, V.I. Corporation's DataView Graphics.

Developers access Nexpert through an easy-to-use Microsoft Windows interface for interactive development and can customize Windows interfaces for interactive applications.

Sophisticated expert-system shells often allow developers to design expert systems that are so complex that even their creators have difficulty understanding the potential interactions between knowledge structures. Nexpert lessens this problem with a utility that clearly displays intricate relationships between rules and frames, decreasing development time and allowing systems to be developed that otherwise would be too complex to debug.

Nexpert's competitive success, however, is due only in part to its C library and its windowing capabilities. Equally important, Nexpert is a sophisticated, full-featured expert-system shell competitive with higher-priced mainframe packages. Nexpert's comprehensive inheritance scheme gives the developer greater control over the inferencing process than many other expert-system toolkits. The shell supports inheritance of frame-based knowledge downward through the rule base in the traditional manner (from parent to child) as well as upward (from child to parent), and it allows the developer to dynamically alter the inference strategy.

Neuron Data designed the shell for both knowledge engineers experienced with shell use as well as domain experts (specialists in a particular field) with no previous AI experience, although in practice, it is a sophisticated tool more appropriate for experienced users. The Nexpert developer, however, does not need to know LISP, a possible advantage over Gold Hill's rival product, GoldWorks (for a review of this product see "The Age of GoldWorks,"

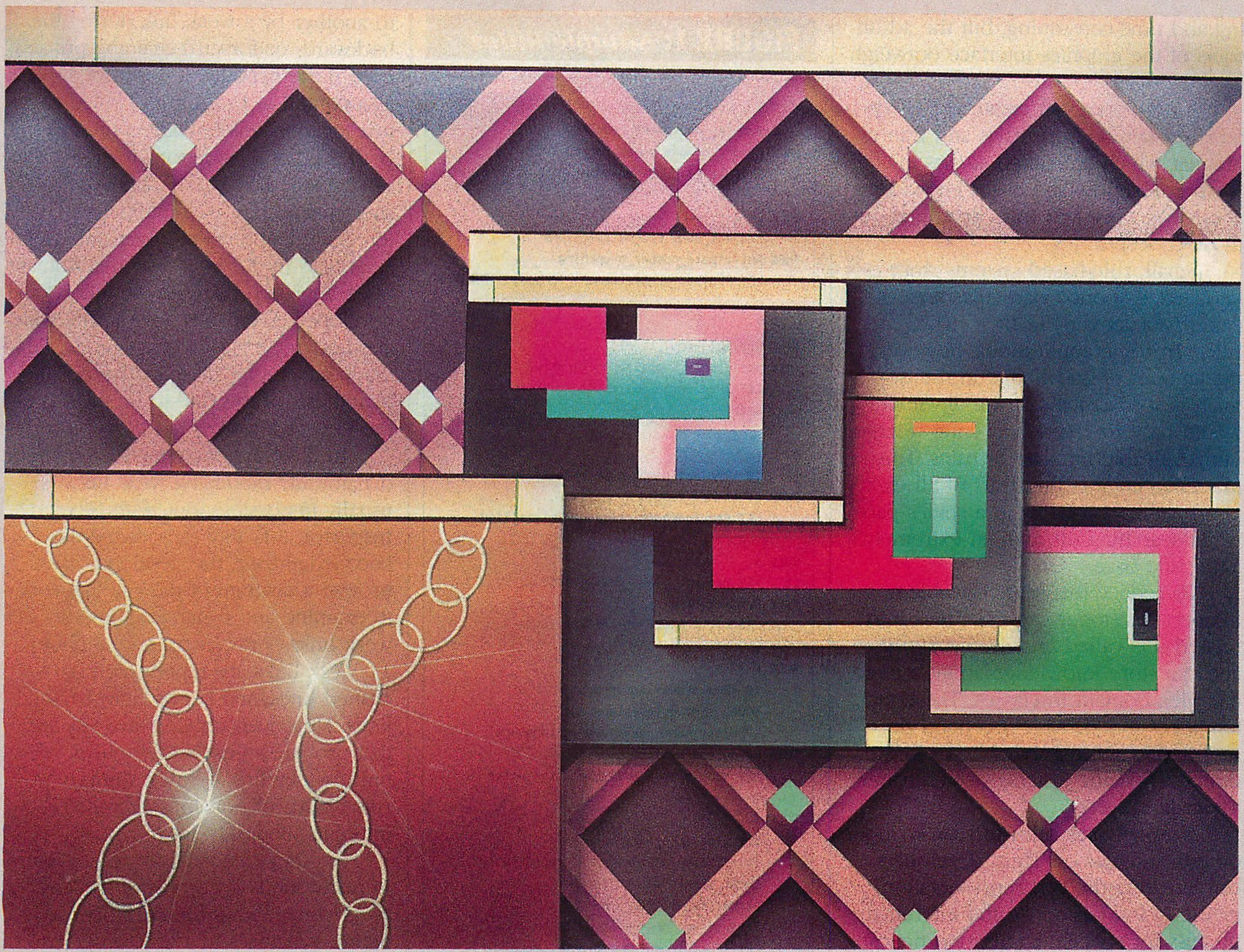


ILLUSTRATION • ANDY LEVINE

Ken Levine, May 1988, p. 68). Nexpert is a good choice for developers familiar only with traditional languages.

Although sometimes mistakenly called a midrange tool, Nexpert has the facilities of high-end mainframe systems, such as IntelliCorp's Knowledge Engineering Environment (KEE) and Inference Corporation's Automated Reasoning Tool (ART), but without the high-end price. Nexpert configured for the IBM PC/AT costs $5,000. Unlike more expensive competitors, systems designers can develop and deliver Nexpert applications on a wide variety of hardware, including the IBM PC and PS/2 (both 80286 and 80386), IBM RT PC and mainframes, Macintosh II and SE, Sun and Apollo workstations, and the entire DEC VAX line. Expert systems developed under Nexpert on one system can be ported easily to other Nexpert environments.

The PC version of Nexpert requires an IBM PC/AT with at least 640KB of RAM (2MB recommended), a minimum of 1MB on a hard-disk drive, and a 1.2MB diskette drive. Other hardware requirements are an EGA and monitor, a bus or serial mouse (Microsoft or Mouse Systems recommended), and an expanded-memory board (2MB of RAM recommended). A runtime version of Microsoft Windows is needed.

Although the program diskettes are not copy protected, Nexpert includes a hardware device that prevents illegal use of the product. The device fits into a serial port and is invisible to other peripherals using the port. Nexpert occasionally checks the device for a unique serial number; if it detects that the hardware device is missing, Nexpert ceases running and exits to DOS.

Many companies large and small have adopted Nexpert. Engineers at Martin Marietta designed a Nexpert application for NASA that runs on an AT and helps scientists evaluate coatings used to prevent frost build-up and to protect the quality of fuel in space shuttle external tanks. COMSAT developed and is now using a Nexpert-based system to help its operations staff configure thrusters on orbiting INTELSAT V spacecraft. The flexibility of the inference process was a prime consideration for the COMSAT developers.

FRAMES OF MIND

The developer starts Nexpert as a Microsoft Windows application. A full-screen window with a pull-down menu bar across the top allows the developer to navigate the shell with selections such as the following: Edit, to access editing windows for knowledge elements such as rules; Expert, to load knowledge bases, start the inference process, or change the inference strategy; Inspector, to display the knowledge base graphically; and Report, to access information about the status of inferencing and knowledge structures.

The Encyclopedia option retrieves lists of existing rules, data, hypotheses, objects, classes, and properties in the form of alphabetically indexed pages, and the Windows option allows the developer to control the display of windows. Any windows that have been created on the screen can be moved simply by dragging or explicitly moving them anywhere on the screen. The windows automatically created by Nexpert are often positioned so that part or all of the information they contain is obscured. Repositioning can be distract-

ing and time-consuming, but the advantages of the graphics interface outweigh its drawbacks.

A developer can create expert systems containing both rules and frames. Frames, which are called *classes* in Nexpert terminology, order knowledge about concepts, and rules reason about those concepts.

Small, rule-based systems store knowledge about a particular area of expertise (domain) in If . . . Then rules. In some applications, however, the amount of knowledge in the domain is so massive that the developer would have to create and enter a large, unmanageable number of rules. The inference engine, the heart of all expert systems, can slow to a snail's pace when searching through an extremely large rule base.

To reduce this search problem, a Nexpert developer can link rules into related sets called *knowledge islands* and can store knowledge about a large, complex domain in classes. These are templates that provide a general description of a category of items in the domain. Specific instances of each item are called *objects*.

Nexpert uses rules to reason about objects and classes. Thus, developers can integrate the two representation methods and customize the inference process for specific application needs. (See "Computerized Reasoning," Tom Arcidiacono, May 1988, p. 44, for a review of both reasoning systems.)

Rules. A developer structures Nexpert rules much the same way as in other shells. The left-hand side (LHS) of the rule is composed of one or more antecedent (if) clauses, which are called *conditions* in Nexpert. The right-hand side (RHS) consists of one consequent, called a *hypothesis* in Nexpert, that can be true, false, or unknown, and optional actions that occur whenever the hypothesis is true. Figure 1 shows several rules from a sample resource-scheduling application developed specifically for this review to test Nexpert's capabilities. (For an explanation of *PC Tech Journal*'s criteria for evaluating expert-system shells, see "Elements of Expert System Shells," Maxine Fontana and Jordene Zeimetz, May 1988, p. 63.)

As in other rule-based systems, the Nexpert developer can express disjunctive (OR) conditions with two rules pointing to the same hypothesis. When all conditions are true, the hypothesis is true and the actions are enabled. To assist the developer in structuring the knowledge base, the shell automatically creates and enters objects for each condition, hypothesis, and action of each rule. The developer later can place the objects into classes and add other features of hypothesis variables to produce a hybrid expert system.

FIGURE 1: *Sample Rules*

```
RULE 1
IF   Special_equipment_required
THEN Allocate_more_money_for_equipment
     EXECUTE RecalculateBudget @STRING=AItasks

RULE 2
IF   Project_requires_calculations
THEN Anticipate_number_crunching
     LET Project_x.development_language  FORTRAN

RULE 3
IF   Project_requires_AI
THEN Anticipate_symbolic_declarative_language
     LET \Project_name\.development_language
     LISP

RULE 4
IF   IS \Project_name\.type classified
THEN Clearance_needed
     LET Requirements.clearance classified

RULE 5
IF   YES Project_needs_definition
THEN Project_name
     EXECUTE Project_definition_tasks

RULE 6
IF   IS <Employees>.assignment none
     EQUAL <Employees>.language
     \Project_name\.development-language
THEN Resources_available
     LET <Employees>.assignment tentative

RULE 7
IF   Yes Clearance_needed
     IS <Employees>.assignment tentative
     EQUAL <Employees>.clearance
     requirements.clearance
THEN Team_selection_finished
     LET <Employees>.name project_name
```

The left side of the rules from the resource-scheduling application shows the elements of Nexpert rules. These rules contain one or more conditions that, when satisfied, cause the hypothesis on the right side to be true so that prescribed actions can occur.

As with all shells, the developer must design the Nexpert rule base with inferencing in mind. Each rule must have at least one hypothesis that is a condition in other rules, and some rules must include conditions that are hypotheses in other rules.

Rules that share data or hypotheses are strongly linked into knowledge islands, a simple way to control the portion of a knowledge base on which inference occurs.

A Nexpert developer also can define *weak links*—relationships between rules that do not share conditions or hypotheses. The inference engine examines the hypothesis of a rule joined to another by a weak link during the backward- or forward-chaining process, even if the hypothesis does not appear as a condition in the set of rules under investigation. Inferencing continues on both sets, as if evidence for the weakly related rule had been obtained. Such shortcuts add a new dimension to inferencing by allowing investigation of sidetracks in the same way that humans often approach complex problems. The developer establishes a weak link with another rule by using the Context Editor to attach explicit information (the hypothesis of the rule to be linked) to the RHS of a rule.

In most expert systems, creating or dynamically modifying weak links is usually impossible. But, with Nexpert's Inspector, a facility for viewing the knowledge base, the developer can browse a diagram of the rule network to examine and dynamically modify the weak links between rules (see photo 1). Weak links are represented by dashed lines, and strong links by solid lines. Moreover, unlike other systems that provide an execution trail of rules only as they fire, Nexpert displays rule-based relationships even before inference begins.

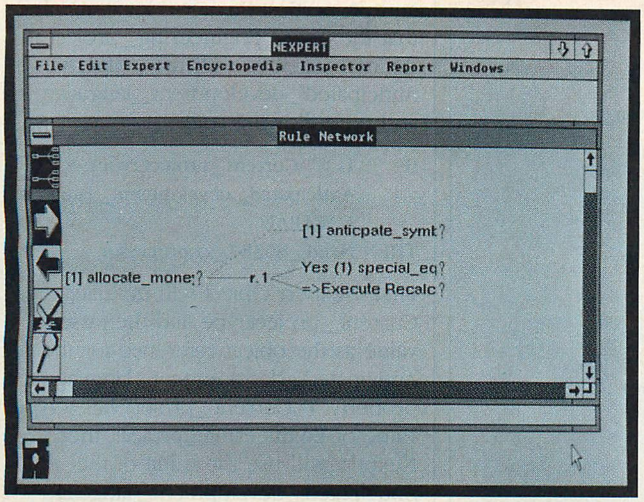
Another Nexpert feature not found in many shells is *constraint propagation*, which allows the developer to define structures in a knowledge base that depend in some way on the values of other structures. One example of such a constraint taken from the resource-scheduling application could be assigning team size for a project based on the project length. For example:

```
IF      Project_duration_changed
THEN    Hypothesis_X
DO      2 + ((1/Project_length_wks) * 10)
        Team_size
```

If a two-week project had to be finished in one week, management could assign extra members to the team. Nexpert will automatically fire this sample rule and recalculate Team_size when Project_length_wks changes. Therefore, Nexpert automatically maintains the constraint that Team_size is defined in terms of the current value of Project_length_wks. This kind of relationship is common in many applications, although usually difficult to define and maintain. In some systems, the developer must write *demons* (callable functions) to handle constraints.

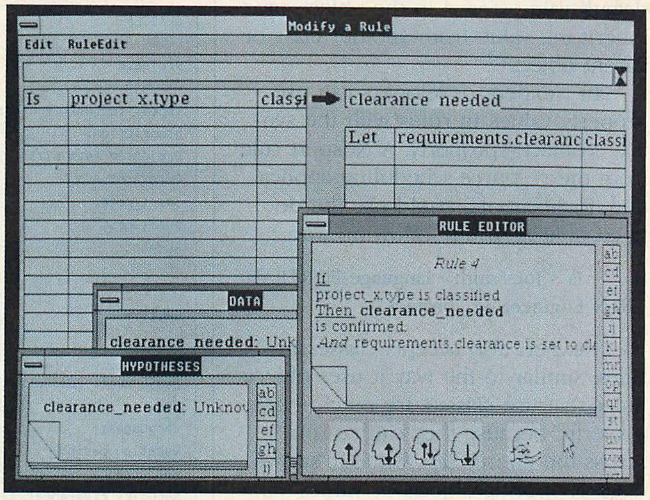
Nexpert cannot handle uncertain data as well as it deals with constraints. Although the system can reason with uncertain data, Nexpert does not have any built-in certainty calculations. A

PHOTO 1: ***Nexpert's Inspector***



The Inspector, one of Nexpert's most sophisticated features, allows the developer to browse the rule or object base at any time. Rules that share elements (connected by unbroken lines) indicate a strong link; rules associated by context (connected by dashed lines) indicate a weak link.

PHOTO 2: ***The Rule Editor***



Nexpert's interactive Rule Editor allows operators (such as IS or EQUAL) and actions (such as LET or EXECUTE) to be selected from pop-up menus available by pressing the right-hand mouse button; expressions are typed in. Rule, Data, and Hypothesis notebooks can be displayed.

developer must use the normal rule syntax to define probability calculations and test any needed *confidence values*, or numbers that represent the certainty of data. For example:

```
IF      Yes Evidence_for_a_theoryA
        <= Confidence_theoryA - 1
        >= Confidence_theoryA + 1
THEN TheoryB
DO      Confidence_theoryB +
          (1 - Confidence_theoryB) *
          (.08 * Confidence_theoryA)
          Confidence_theoryB
```

In this case, the system must explicitly test the confidence in theory A and must explicitly calculate the confidence in theory B if used later. (The developer could define a function to perform the calculations, making the rule less cluttered.)

This method of supporting probabilistic reasoning places too much responsibility on the developer for details that are difficult to maintain consistently. Nexpert should provide default functions as well as user-defined probability functions.

Classes and objects. Nexpert, like other hybrid shells, takes an object-oriented approach using a hierarchy of both classes and objects. Each class has a name, lists of subclasses, and properties; each object has a name, a list of classes to which it belongs, a list of subobjects from which it is constructed, and properties. The properties of Nexpert classes and objects (like those of frames and instances) describe the characteristics of the class and object.

Property slots hold values; the property Employees_languages, for example, could hold the values C, FORTRAN, Pascal, or Ada.

Figure 2 shows the internal structures of classes and objects in the sample application and their relationships. The Employees class lists characteristics (properties) of a typical employee (such as Name and Languages) along with default values. The object, JoeSmith, is an instance of Employees because it refers to a specific employee.

The developer can assign property values to an object, such as FORTRAN for the Languages property of an employee's object. Nexpert also can assign a value on the fly during inferencing; or values can be inherited from other objects or the class. In the Employees class, for example, the property Security_clearance might have the value 1 (if all programmers in the department must have low-level clearance), while the property Assignment might be empty.

In fact, one of Nexpert's most important features is its hierarchical network of classes and objects that supports downward inheritance (inheritance of property values from parent class or object to child), upward inheritance (inheritance of property values from child to parent), and multiple inheritance (inheritance of property values from multiple classes or objects). Objects inherit default property values from the class unless the developer assigns them values or the inference engine concludes values for them.

The developer can customize the source and timing of inheritance (and inference) by attaching information to the property using *meta-slots.* These are system properties the developer defines for each property of a class or object. Nexpert allows as many as seven meta-slots for each property.

When an object can inherit a property value from more than one class or parent object, for example, the developer uses the property's inheritance category to specify which parent has a higher priority. The Inheritability meta-slot controls whether or not other objects can inherit a given property. With the If-change meta-slot, the developer defines functions (demons) for the system to perform whenever the value of a property is changed; the Prompt-line meta-slot provides a prompt string for user-entered values.

The Nexpert developer also can place each property in a particular inference category to prioritize data for consideration during inferencing using the Inference Category meta-slot. The default for this category causes the inference engine to evaluate rules containing the property value in order of entry. Developer-defined priorities can resolve conflicts when two rules are true simultaneously.

When Nexpert encounters an unknown property value, the Order-of-sources meta-slot determines how to proceed. If the object's property is in a rule the system currently is testing but the value of the property has not yet been determined, Nexpert has five al-

ternatives: query the user, call an external procedure, search a database, use a default value stored in the object, or inherit the value from another class or parent object.

In Nexpert, developers can use property values in rules with the syntax, <object>.property. A Nexpert rule from the resource-scheduling application, for example, could use the defined objects in the following way:

IF Is <Joe-Smith>.language FORTRAN
THEN Engineering_project

Nexpert also accepts classes in rules, similar to the way it uses objects. Rules that use classes are much more powerful because they can reason across the entire class without knowledge of specific objects or values within the class. Assume, for example, that a rule is needed to determine whether any programmers have security clearances less than level 2, and to disqualify them from a project by setting their Project_status property value to "Disqualified."

One method of accomplishing this is to create a separate rule for each employee object in the Employees class. A more efficient method uses classes within rules. The developer does not need to encode specific knowledge about all the members of the class. (This might be impossible anyway, because objects and classes can be created and destroyed dynamically in Nexpert.) Nexpert supports the following syntax:

IF <Employees>.clearance 2
THEN Let <Employees>.Project_status "Disqualified"

Thus, the project status of any employee objects whose security clearance is less than level 2 will be set to "Disqualified." The system then uses objects found on the LHS of the rule in the assignment on the RHS, similar to the way in which Prolog can instantiate variables in one part of a clause and use them in a subsequent part.

Substituting classes for objects is called *pattern-matching* in Nexpert, because the rule actually is trying to match specific object names against the more general pattern provided by the class name. Nexpert, however, cannot duplicate the type of true pattern-matching that is possible in LISP-based tools. For example, developers cannot easily implement natural-language programming using Nexpert. The system cannot easily read a sentence of text as input and then fire rules on general patterns of text within the sentence.

FIGURE 2: ***Classes, Objects***

```
CLASSES:

Projects

Type: (default = classified)
Description:
Projected_team_size:
Duration:
Start_date:
Deadline:
Budget:


Employees

Name:
Assignment: (default = none)
SS#:
Languages:
Vacation_period:
Performance_rating:
Security_clearance:
Sex:
Date_of_hire:
Project_status:


OBJECTS:

Project_X

Name: Hydrodynamic_Vehicles_Project
Type: Secret
Description: "Preparation of software
  to analyze designs for vehicle compo-
  nent prototype. Anticipate use of AI
  and numerical analysis techniques."
Projected_team_size: 2
Anticipated_development_language: LISP
Start_date: 890103
Deadline: 890701
Budget: 270000.00


Joe-Smith

Name: Joseph Hilary Smith
Assignment:
SS#: 555 12 1234
Languages: C
Vacation_period: 890115 - 890201
Performance_rating: 5
Security_clearance: 5
Sex: Male
Date_of_hire: 830101
Project_status:


Christine-Flynn

Name: Christine Margaret Flynn
Assignment:
SS#: 555 44 4321
Languages: LISP
Vacation_period: none
Performance_rating: 8
Security_clearance: 1
Sex: Female
Date_of_hire: 880601
Project_status: Disqualified
```

In Nexpert, templates that provide general information about items in the domain are called classes, specific instances of each item are objects. Both are further characterized by properties, which may have values and meta-slots (directions for behavior) that are associated with them.

Nexpert allows rules to use values of properties to access other objects and properties. Suppose, for example, that the object Engineering_project is defined together with the property Anticipated_development_language and the following rule:

IF Is " "\Current_project.type\.
Anticipated_development_language FORTRAN
THEN Need_80387_coprocessor

First, Nexpert Object will evaluate Current_project.type and then use its value as the object reference for the Anticipated_development_language property. If Current_project has a type value of Engineering_project, then Nexpert will use the value of the Anticipated_development_language property for the Engineering_project object for the test.

The CreateObject operator dynamically creates and eliminates objects, modifies objects, or establishes hierarchical relations with additional classes. The following rule, for example, causes the object My_PC to be an instance of LISP_machine as well as PC_class, allowing it to inherit the additional properties of objects in the new class:

IF Yes LISP_board_added_to_PC
THEN PC_now_LISP_machine
THEN CreateObject My_PC LISP_machine

The CreateObject operator is a powerful and unique way to build frame lattices because the developer can give objects multiple parents from which to inherit properties and values. Runtime systems have the power to control inheritance by dynamically establishing these relations between objects and through inference categories.

Because it is a highly interactive system, Nexpert does not insist on having complete definitions of frame-based information. Instead, the Nexpert system supports an incremental, interactive approach to building knowledge structures. The developer often defines meta-slots, for example, late in the development cycle during debugging of the inference process.

SEEING IS BELIEVING

The sample application, developed for this article, is designed to assist management in scheduling resources in a large corporation. It is a good example of an expert system that uses both rules and classes.

A common task in contract programming shops is the assignment of software engineers to projects. After

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CGA	320x200	16/64
MDA	720x348 640x400	

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LINES OF TEXT	132x44	132x25	132x44	132x60	132x60	132x60	132x60
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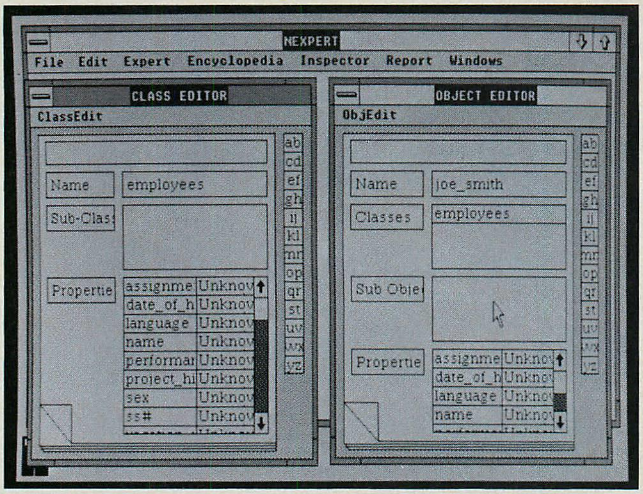
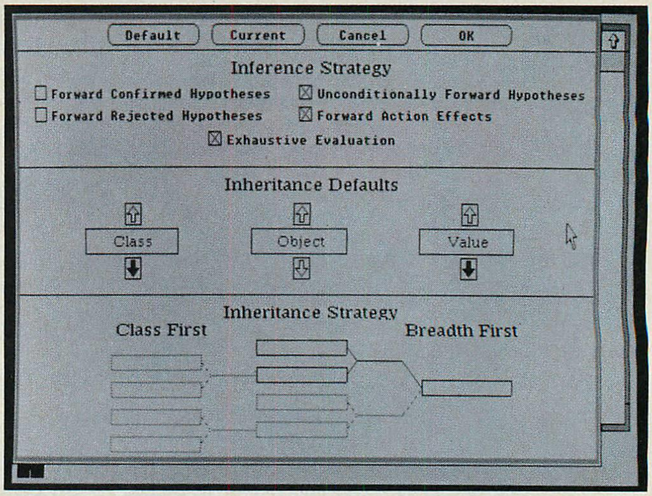
PHOTO 3: ***The Class and Object Editors***



Moving and sizing windows allows several windows to be displayed on the screen simultaneously. Developers enter both classes and objects interactively in Nexpert, using an editor that presents an appropriate screen.

PHOTO 4: ***Changing Inferencing Strategies***



Another high-end feature that distinguishes Nexpert is its inference flexibility. Developers can assign default strategies for inferencing during development but can change these interactively at any time using the Strategy menu.

becoming familiar with the requirements of a project, the manager or project leader chooses members of a development team according to factors such as general experience, expertise with specific languages or tools, and availability.

A manager also must consider less tangible factors such as the ability to work with other members of the development team, preference, corporate policy, appearance, temperament, and past performance. In a large organization with many pending projects and large numbers of personnel, this scheduling task can be immensely complex and expensive.

A well-designed expert system could provide cost-effective assistance with this process. Using several sources of data—including personnel records, past project histories, and project descriptions—and applying a set of rules that captures the expertise of a human scheduler for considering all factors affecting the assignment, the expert system could suggest appropriate programmers for specific tasks. Figures 1 and 2 show a sample of the rules, classes, objects, and properties from the sample application.

Objects in the Projects class have eight properties but could have others if they also are members of other classes. Objects in the Employees class have ten properties.

Two objects (Joe-Smith and Christine-Flynn) are instances of the Employees class, and the object (Project_X) is an instance of the Projects class. In Nexpert objects, property values (such as Name and Performance_rating) can have only string, numeric, or Boolean data types (they cannot be lists). This is a liability in some cases. Because some programmers are proficient with more than one language, for example, it would be convenient to keep a list of primary languages attached to each Employee object. Unfortunately, Nexpert forces the developer to solve this problem, although Neuron Data plans to address this in future versions.

One way to work around this inability to use lists in properties is to keep the list in a string, although the developer must provide appropriate functions to operate on the string. A slightly more complex (and less efficient) alternative is to create an object called Primary_languages containing as many subobjects as there are languages in the list. Each subobject would have the value of one language.

Nexpert's inheritance scheme is one reason the system is a good choice for developing a resource-scheduling application. Classes and objects in the sample application can use downward inheritance to inherit property values from the objects and classes of which they are a part.

If the project requires three distinct phases for completion, for example, the Nexpert developer can create three subobjects for the project with the same properties as the project itself. Each subobject can inherit the value of the project's Type property from the parent object. In fact, any of the project properties whose Order-of-sources meta-slot is given the value Inheritable-down will be assigned to the corresponding properties of the subobjects.

Upward inheritance is a very powerful tool because it enables some features of objects to be determined largely by the features of the subobjects, instead of the other way around. Nexpert is one of the few shells to offer this feature.

The developer can achieve upward inheritance in a similar way to downward inheritance by setting the Order-of-sources meta-slot for a property to Inheritable-up. The object Project_X, for example, could inherit a Type value from any of the subobjects whose Type property has Inheritable-up as the value of its Order-of-sources meta-slot. Because of this complex inheritance structure, Nexpert rule bases are much more difficult to read than those of simpler systems such as Texas Instrument's Personal Consultant Plus (for a review of the latter product, see "Sophisticated Expert," Susan J. Shepard, July 1988, p. 106). Nexpert developers, however, can see the relationships by using the Inspector.

The developer can write simple rules such as Rule 2 in the resource-scheduling application, which concludes that number crunching will be needed if the project requires calculations. More complex rules, such as Rule 5, dynamically create an object to contain all of the property values of the project under consideration by executing an external subroutine to create a new object based on that name and give values to some of the object's

properties wherever possible. The CreateObject operator achieves the same result.

Other rules can set an object's property value. In Rule 3, for example, the project object's property value, Development_language, is set to LISP when the system discovers evidence that project programmers will need in order to use AI.

The developer also can use pattern-matching in rules to create a list of objects with given properties on the LHS of a rule and use the list on the RHS, as illustrated in Rules 6 and 7. Rules also can call external routines. Rule 1 calls a routine to recalculate the budget if the project will require special equipment. The string value AItasks (set previously) is passed to the routine that updates the Budget property of the Project_X object.

External routines in the LHS of a rule can provide data and return either a true (1) or false (0) value to the inference engine. A rule can test, for example, to see whether a particular key word appears in the project object's Description property and, if so, can confirm an hypothesis regarding the anticipated development language. The system passes the project's description string as an argument to the external routine (or executable file).

The external routine cannot return values other than true or false directly to the LHS of a rule. One way to get around this limitation is to create a new object from the routine and assign the value to the new object.

Although returning lists of values for assignment or use by a corresponding list of objects is often useful, Nexpert does not permit external routines to return lists. To return lists, the developer must create a new object for each list item. However, the system can pass a list of objects created by pattern-matching to an external routine.

Rule 6 selects all of the objects of the Employees class whose Assignment property has the value none (employees not yet assigned). Then the rule selects only those objects whose Language property is the same as the project's development language. This process is analogous to the creation of a selection set with database query languages such as SQL. The RHS of Rule 6 assigns a value to the Assignment property of each object in the previously created list.

Knowledge islands focus the inference engine on specific sets of rules; weak links relate rule sets. The developer created a weak link between Rule 3 and Rule 1, for example, because projects using LISP sometimes require special computer equipment or software support. When Rule 3 fires, it confirms that the project requires a symbolic language and specifies through the weak link that the system should investigate Rule 1. The inference engine uses backward chaining in order to look for the rules confirming Allocate_more_money_for_equipment.

The group of rules explored as a result of the backward chaining on Rule 1 forms another knowledge island. Although the project may not require special equipment, the inference engine will explore the hypothesis because Nexpert inferred that LISP should be the development language. Shells that do not support weak links would be less efficient at finding the proper sequence of inferences to occur.

Nexpert rules can retrieve data from existing databases either to query the information or to map it into objects. If information about each employee is in a dBASE III PLUS database, Nexpert can map information from

each record into a corresponding object in the Employees class or can place field values in object properties.

Entering rules. Entering rules is highly interactive in Nexpert. The developer defines rules using the Rule Editor menu by selecting the Editor option from the main menu. Nexpert presents a rule-entry screen, the LHS for the condition, the RHS for the hypothesis, and optional actions.

The developer selects a condition's operators from a pop-up window accessible by positioning the cursor in the operator box on the rule-entry form and clicking the right-hand button on the mouse. The developer then clicks on an expression box and uses Edit Line, a text-entry bar at the top of the form, to enter and edit expressions and hypotheses.

The developer enters optional actions through a pop-up menu, which contains options such as Creating an object (CreateObject), Loading a knowledge base (LoadKB), Assigning a value to a property or variable (Let), and Changing the inference strategy (Strategy). Photo 2 shows the Rule Editor window, the Data and Hypothesis notebooks, and the rule-entry screen.

The developer can check the syntax of the current rule by accessing the RuleEdit option from the Rule Editor menu bar. If the rule is correct, OK will be highlighted; selecting OK saves the rule and exits the Rule Editor. Otherwise, the Check option highlights the incorrect elements of the rule.

Such a highly interactive rule-editing environment can be tedious for experienced knowledge engineers who are in a hurry to encode large numbers of simple rules—typing the entire condition is often easier. This environment, however, is an excellent method for beginners and for developers who want to build rules through trial and error. With practice, the interaction becomes faster.

Entering classes. As with the rule-building process, Nexpert has a variety of methods for creating classes and objects, but the Class Editor and Object Editor (accessed from the Edit Menu) are the most direct. The Object Editor is a form with boxes for the object's name, classes, subobjects, and properties.

The developer can enter information about the object in any order and can scroll the boxes to view large lists of classes or subobjects. Entering classes and subobjects requires two clicks on the mouse—the first click selects the type of information, the second click accepts the specific data. Unfortunately, this two-click process is somewhat cumbersome.

The developer enters property names in the same way as classes and subobjects. Photo 3 shows the class and object editor windows in which the Employees class and Joe-Smith object have been defined.

Two boxes appear beside the name when entering the property name. The developer attaches a value to the property by clicking on the first box and typing the value. To add meta-slots and their values, the developer clicks on the second, smaller box to display the Meta-slots Editor window (which is easily accessed from Inspector and Notebook windows).

With the Meta-slot Editor—an extremely powerful feature of Nexpert—the developer can control precisely how Nexpert uses properties and values during the inference process. The Meta-slot Editor has boxes for the Inheritance and Inference categories, numerous options for how the property can be inherited by others, the order of sources for the value, the ac-

Cocaine lies.

After nearly a decade of being America's glamour drug, researchers are starting to uncover the truth about cocaine.

It's emerging as a very dangerous substance.

No one thinks the things described here will ever happen to them. But you can never be certain. Whenever and however you use cocaine, you're playing Russian roulette.

You can't get addicted to cocaine.

Cocaine was once thought to be non-addictive, because users don't have the severe *physical* withdrawal symptoms of heroin—delirium, muscle-cramps, and convulsions.

However, cocaine is intensely addicting *psychologically.*

In animal studies, monkeys with unlimited access to cocaine self-administer until they die. One monkey pressed a bar 12,800 times to obtain a single dose of cocaine. Rhesus monkeys won't smoke tobacco or marijuana, but 100% will smoke cocaine, preferring it to sex and to food—even when starving.

Like monkey, like man.

If you take cocaine, you run a 10% chance of addiction. The risk is higher the younger you are, and may be as high as 50% for those who smoke cocaine. (Some crack users say they felt addicted from the *first time* they smoked.)

When you're addicted, all you think about is getting and using cocaine. Family, friends, job, home, possessions, and health become unimportant.

Because cocaine is expensive, you end up doing what all addicts do. You steal, cheat, lie, deal, sell anything and everything, including yourself. All the while you risk imprisonment. Because, never forget, cocaine is illegal.

There's no way to tell who'll become addicted. But one thing is certain.

No one who is an addict, set out to become one.

C'mon, just once can't hurt you.

Cocaine hits your heart before it hits your head. Your pulse rate rockets and your blood pressure soars. Even if you're only 15, you become a prime candidate for a heart attack, a stroke, or an epileptic-type fit.

In the brain, cocaine mainly affects a primitive part where the emotions are seated. Unfortunately, this part of the brain also controls your heart and lungs.

A big hit or a cumulative overdose may interrupt the electrical signal to your heart and lungs. They simply stop. That's how basketball player Len Bias died.

If you're unlucky the first time you do coke, your body will lack a chemical that breaks down the drug. In which case, you'll be a first time O.D. Two lines will kill you.

Sex with coke is amazing.

Cocaine's powers as a sexual stimulant have never been proved or disproved. However, the evidence seems to suggest that the drug's reputation alone serves to heighten sexual feelings. (The same thing happens in Africa, where natives swear by powdered rhinoceros horn as an aphrodisiac.)

What is certain is that continued use of cocaine leads to impotence and finally complete loss of interest in sex.

It'll make you feel great.

Cocaine makes you feel like a new man, the joke goes. The only trouble is, the first thing the new man wants is more cocaine.

It's true. After the high wears off, you may feel a little anxious, irritable, or depressed. You've got the coke blues. But fortunately, they're easy to fix, with a few more lines or another hit on the pipe.

Of course, sooner or later you have to stop. Then—for days at a time—you may feel lethargic, depressed, even suicidal.

Says Dr. Arnold Washton, one of the country's leading cocaine experts: "It's impossible for the nonuser to imagine the deep, vicious depression that a cocaine addict suffers from."

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tions to be taken when the value is changed, and the prompt to be used if Nexpert queries the user for the value.

An interesting feature of Nexpert is the automatic inheritance between classes and objects. When the developer adds new properties to a class, Nexpert automatically adds this information to any defined objects of the class (unless the order of meta-slots prevents this). When the developer adds the property Language to the class Project, for example, Nexpert automatically adds the property to the object Project_X.

Viewing knowledge structures. The developer can display the knowledge base in a number of helpful ways. After a rule has been saved, the Rule Notebook window appears on the screen (also available from the Encyclopedia menu in the Nexpert window), which presents a series of windows showing the rules in alphabetic order. The developer can flip sequentially through the windows using a mouse.

Notebooks also exist for data, hypotheses, objects, properties, and classes and contain alphabetic indexes for random access. The developer accesses a particular piece of knowledge by clicking on the pair of letters corresponding with the first letter of the name of the item being sought. To view the hypothesis Clearance_needed, for example, the developer selects the Hypothesis notebook and clicks on the letters C-D.

Besides notebooks, Nexpert offers graphics tools for viewing the knowledge base. To look at the rule network, the developer selects the Browse Rule Network option from the Inspector menu. The Rule Network window (see photo 1) contains a series of icons along the left edge for moving through and changing the display of rule interrelationships. Nexpert initially displays a random portion of the rule network.

To display the rule whose hypothesis matches the condition of a selected rule, the developer first clicks on the left-arrow icon (the cursor changes to a left arrow) and then on the current rule. After clicking on the right-arrow icon (the cursor changes to a right arrow), Nexpert displays the rule whose condition matches the hypothesis of the current rule. When the developer clicks on a condition or hypothesis, Nexpert displays all the associated rules, thus displaying all the links between the rules.

A magnifying-glass icon focuses the display on a particular item in the network, such as a rule or hypothesis.

Other icons simplify the display by removing items and accessing additional rules, data, and hypotheses.

The other Inspector menu selections include Overview Rule Network, which allows the developer to start with a very high-level view and subsequently focus on a particular item; Current Rule, which initially focuses on the current rule; and Change Rule Settings, which controls display attributes such as font and color.

The Nexpert developer can view frame structures with the Browse Object Network menu, which is very similar to the Rule window. Selected from the Inspector menu, it shows relationships between classes and objects, objects and subobjects, and classes and subclasses.

Inspector windows are useful and easy to use, although frequent repositioning is necessary even for a very small knowledge base.

Lower-end expert systems do not have this type of graphics display. After some practice with Nexpert's displays, experienced knowledge engineers will be able to predict and debug complex reasoning pathways that otherwise would be impossible to chart.

The inference process. Unlike most other shells, Nexpert reasons using a number of strategies and has several options for beginning the inference process. Each knowledge base has a default reasoning strategy, but the developer can change this and choose between forward (event-driven) processing, backward (goal-driven) processing, or a combination of the two.

Additional inference pathways are identified by keeping a list of agendas, which are the hypotheses of successfully fired rules. The system adds a new hypothesis to the list of agendas when a rule in which it is contained has its conditions satisfied indirectly by other backward-chaining rules. In Nexpert, any rule fires forward if the system examines and satisfies its conditions while trying to fire other rules. When the rule is satisfied, Nexpert adds the hypothesis to the list of agendas.

The user starts the inference process by selecting KNOWCESS from the Expert menu, which displays the Session Control window. Nexpert creates a list of initial hypotheses and begins to process the rules and objects.

At the same time, the system overlays several other windows on the screen to display information such as hypotheses currently under investigation (the Hypothesis window), transcripts of any values the system has

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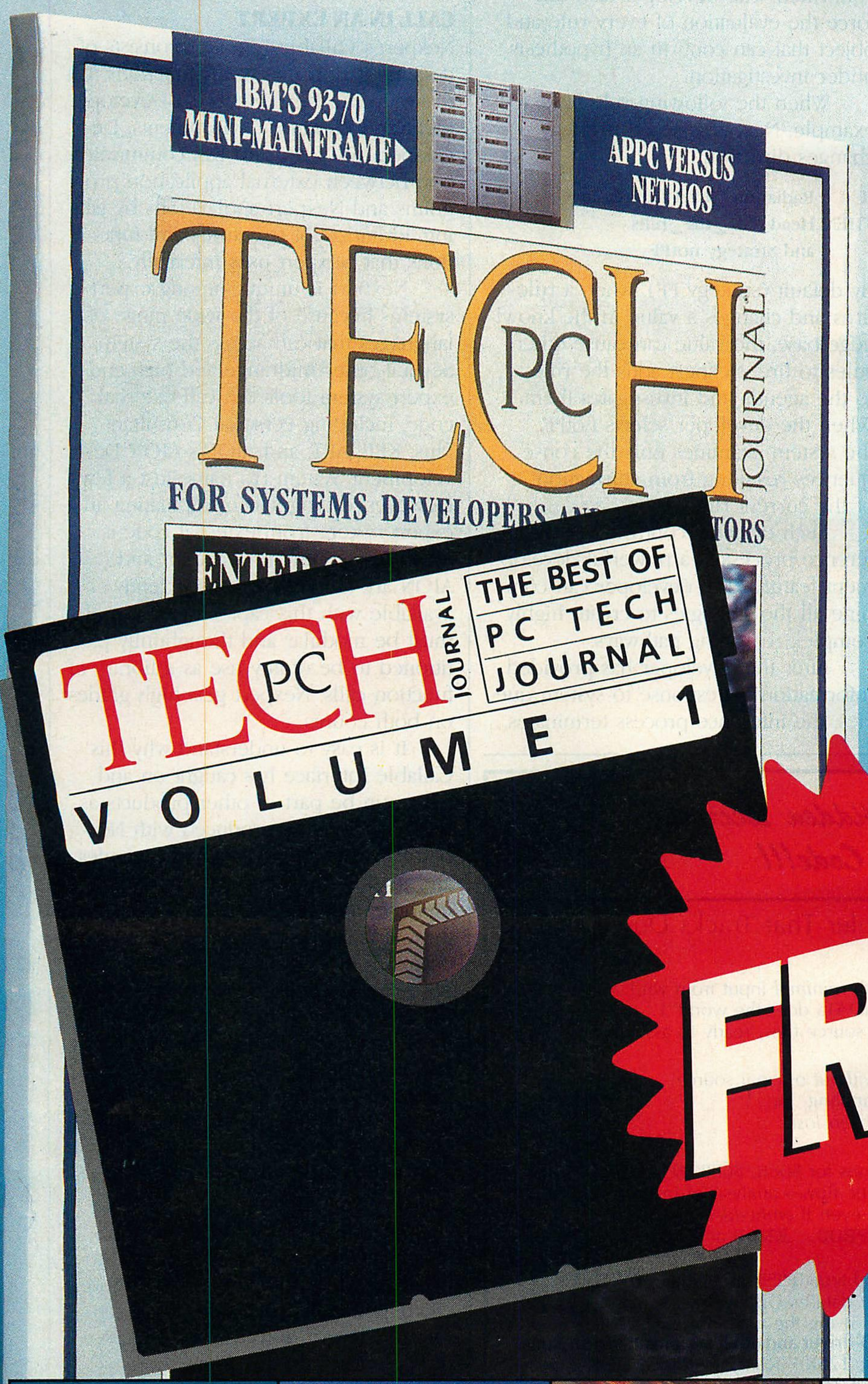

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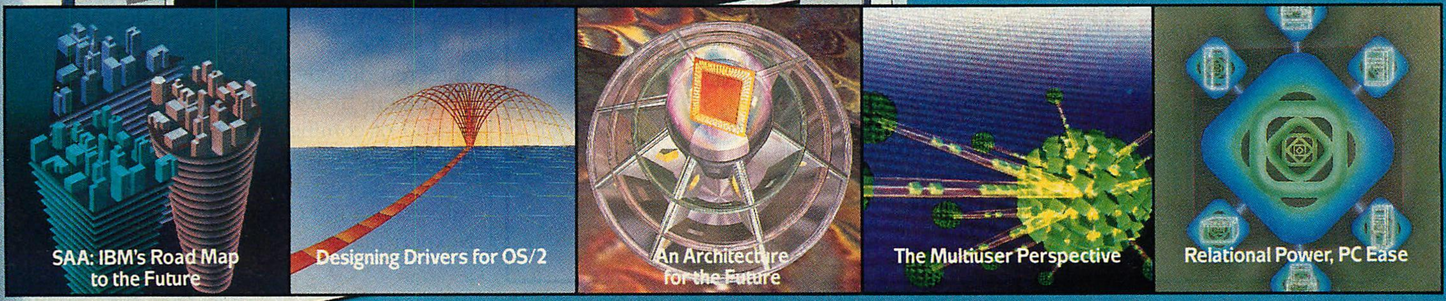

obtained or altered (the Transcript window), the rules currently under investigation through backward chaining (the Rule window), and any concluded hypotheses (the Conclusions window). The user can access these windows throughout the inference process.

The user can interrupt the inference engine to *volunteer* (input) information to the Nexpert system regardless of whether the new data are relevant to the rules and hypotheses currently under investigation. The user can start a forward-chaining process, for example, by entering all information about a problem and then letting the system fire every possible rule to develop hypotheses.

The user can *suggest* one or more hypotheses for backward chaining that the system uses as a starting point for the inference process, regardless of whether the system currently is investigating those hypotheses. After studying the initial or suggested hypotheses, the system then identifies other hypotheses worth examining.

Nexpert's flexibility and user interaction sets the inference engine apart from many others in which rules only can fire blindly in a single strategy. The developer can use Nexpert's Strategy menu (see photo 4), for example, to fire only the rules concerned with confirmed hypotheses, examine only data that would reject an hypothesis, or examine all data regardless of whether the associated hypothesis is rejected or confirmed. The developer also can force the evaluation of every rule and object that can confirm an hypothesis under investigation.

When the following rule fires, for example, Nexpert's search strategy changes direction:

```
IF      Radiation_level_increasing
THEN Head_for_the_hills
        and Strategy notPF
```

By default (strategy PF), when a rule fires and changes a value in the knowledge base, the value can cause other rules to fire. Nexpert adds the rules to the agenda and investigates them. When the developer selects notPF, the system examines only the consequences resulting from affirmation of the current rule.

Such dynamic control over the inference process is a powerful development feature. The developer can combine all the strategies to create highly complex reasoning pathways.

After the developer has provided information in response to system queries, the inference process terminates. The results of the inference session are displayed in the Conclusions window. Each hypothesis investigated is either rejected, confirmed, or already known to be true.

CALL IN AN EXPERT

Nexpert's Callable Interface consists of documentation into the C functions that make up the Nexpert Object Development and Runtime Environments. Developers use it to establish communication between external application programs and Nexpert applications by taking advantage of structures and functions that Nexpert uses internally.

Nexpert is unique among expert systems because of the wide range of languages that can access the system. Several other midrange and high-end expert system tools can call external code, including Personal Consultant Plus, KEE, ART, and AION's AION Development System (to name just a few). However, calling and manipulating an expert system from external code is much less common—Nexpert and AION are among the few currently available with this capability. The tool must be modular and thoughtfully partitioned to be of any use as a library of function calls. Nexpert gets high grades on both counts.

It is easy to understand why this Callable Interface has caught on and will soon be part of other products as well. Applications produced with Nexpert can trigger external code in rules and in slots (in the same way that methods are called in GoldWorks), but they can also be triggered by events occurring within the system. The developer can insert user-written functions for specified conditions in place of those that normally would be called by Nexpert. Classes and objects can inherit functional attachments. By monitoring internal states of objects and agendas at given times, external processes even can alter inference strategies in response to external events.

The ability to call external code also makes it easier for developers to make expert-system applications more efficient. Other processes can be activated in response to the verification of hypotheses. In a realtime systems-control environment, for example, the data for Nexpert's objects could be volunteered directly from monitoring equipment by calling external functions instead of coming from the usual volunteering windows.

Developers have at least three ways to use the Callable Interface. The Nexpert functions can be called directly

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as exported C functions by external code; external code can "trap" specific Nexpert functions and declare their own replacements;'or some standard messages can be passed between other Windows applications and Nexpert using Microsoft's dynamic data exchange (DDE) protocol (a system for setting up standard messages to be passed between locations, using Windows as a postal service).

A C library of Nexpert functions does not exist yet for the PC platform. Every function that can be used externally is explicitly exported by Nexpert. Each function is documented in the user's manual.

An application can make direct calls to Nexpert's C functions, although these functions will differ slightly according to underlying hardware. This direct-call method is, however, still the most uniform way to implement external calls across each of the different Nexpert Object platforms. In addition, Neuron Data provides a set of VAX/VMS universal symbols specifically for the DEC environment.

The Callable Interface includes C functions to initialize, start, stop, and resume sessions; query or change knowledge structures; and change the list of hypotheses or agendas.

Making a direct call to a Nexpert function requires the system to use internal Nexpert functions and structure definitions, which must be obtained from the NXPDEF.H include file. Functions are available either by linking to their addresses or by declaring them to be external. Each such callable function is well-documented.

To make a direct call to a Nexpert function, the function must be defined and, in most cases, passed the address of an internal Nexpert structure and a predefined code. Functions can return an integer "pass" or "fail" (in keeping with C convention), and a function is available (NXP_Error) to retrieve more information in the event of failure.

Message-passing is an option for Nexpert users only on AT-class machines. Microsoft Windows provides the message-passing environment between its applications using the DDE protocol. Passing messages between an application and Nexpert requires the usual calls to Windows functions for obtaining the respective window handles of the two applications and setting up records to contain the message parameters. Nexpert includes a set of predefined message identifiers (short integers). Messages can be sent and posted to duplicate most of the functionality of direct C calls.

The developer can set up external routines to take the place of Nexpert functions with either a message or a direct C call. On the AT, it can be easier for the developer to use messages to set handler functions.

Nexpert can convert direct-access calls into message-passing code, which is completely transparent to the user's code. Applications can use this feature to work entirely with C functions and structures, while taking advantage of the convenience and efficiency of DDE under Windows.

THE RUNTIME ENVIRONMENT

A Nexpert application developed in one hardware and software environment can be delivered and run in a considerably different environment. Moreover, the applications need not use the Microsoft Windows interface—the developer can customize the interface to suit the application.

Nexpert's Screen Builder is a menu-based tool for designing data input forms to organize, present, and

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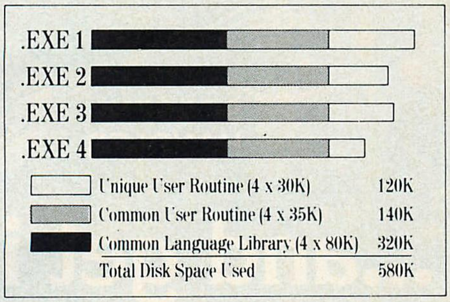
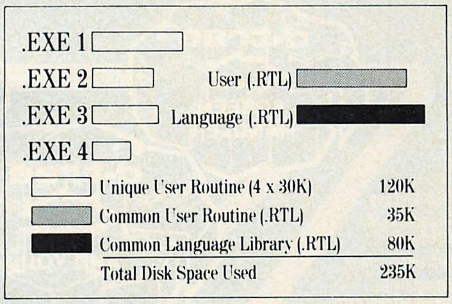


Program = 235K when linked using .RTLink.



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prompt for data. The developer can put form definitions in a file that can be referenced by rules; the system displays forms when they are referenced by a firing rule during an inference session.

A form consists of controls such as string constants, empty text-input boxes, and predefined choices. Controls for input data are associated with objects and their property values. Reports are similar, except they display object values on a screen after the inference process is complete.

The Screen Builder's strength is its simplicity—it is relatively easy to use, even for a beginner. The developer can control small details, such as borders, color of text, and the spacing of items on the screen, and can associate entire files of help text with the screen, making the runtime application very flexible even after delivery.

The developer can edit form files, conveniently stored in a documented ASCII format, with a text editor. Experienced users who find menus tedious will appreciate this feature, although the structure and syntax of the file is relatively complex.

The Screen Builder does have at least one drawback in its type-checking mechanism. For Nexpert to check data values entered by a user, an object (corresponding to a control) and a mask are required to determine the type of value the system needs. The mask values are numeric and difficult to remember.

Using the Nexpert Object Runtime System (NORT), the developer can define in detail how an application will run and can design an interface that is visible to the client (a visible interface is not required).

When a Nexpert application runs, several actions occur: the Screen Builder loads knowledge bases, volunteers some information automatically, displays data-entry screens designed by the developer, and can display the results on a report when the inference process is complete. The system can suggest hypotheses for consideration and determine where to transfer control on completion—to an external routine or back to Nexpert.

Special files control the mediation of input, inference, and output in the runtime application. NORT includes a screen-editing tool to build the first file of screen definitions, used by Nexpert at runtime to show forms. The developer must create a Control File containing commands for loading a knowledge base, selecting behavioral features of the knowledge base, and controlling

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PROGRAMMING PRODUCTIVITY TOOLS

ESSENTIAL C UTILITY LIBRARY

400 Functions, 30¢ Each

You've probably seen the speed and power of Essential's C function library without knowing it. Software greats have been using it for some time to give today's top products pizazz and panache.

Now grown to 400 functions Essential produces pop-up menus, save and restore screens and windows to disk or memory in as little as 1/10th second, and the fastest video output available. Library has a complete set of 50 business graphics functions, 40 string handlers, 28 functions for printers, 18 for mice, 11 for time and date. DOS interfacing functions offer disk error trapping, directory and file management. Everything in source, including sample programs that demo library functions. We have versions with pre-built libraries for all well-known C compilers, and a source code librarian is supplied for rolling your own.

	List:	PC Express
C Utility Library	**$185**	**$119**
Essential Graphics	**$299**	**$225**
Essential Communications	**$185**	**$125**
with Breakout Debugger	**$250**	**$189**

C-TREE & R-TREE

B-Tree File Manager Now Has Report Generator

c-tree: The only major b-tree file manager with network support in the standard low-cost version. c-tree™ gives you record-locking routines for DOS 3.1/3.2, UNIX and XENIX, and it even comes in C source code, yet there are no royalties. Source sticks to K&R, so c-tree is portable. Tests in many environments prove it.

Permits any number of keys for a data file—alpha, numeric, even floating point. Handles files with varied record lengths, multiple keys in one index file. Both high level and decomposed functions. It's the works.

r-tree: Adds the ability to produce ad hoc reports from files maintained by c-tree (v. 4.1 and up). Link a file description to the r-tree™ library, and use any text editor to write report scripts with no further C coding. Reports can access data in several files, select on criteria, join findings into new logical records, sort them, calculate new fields and columns, tabulate by control breaks. Comes in source, same portability as c-tree, and fits any compiler.

	List:	Ours:	Combined:
c-tree:	**$395**	**$299**	**$499**
r-tree:	**$295**	**$235**	

WINDOWS for DATA

M'soft Windows Compatible

"Onlt one package can be easily recommended" said *Computer Language* (June '87) reviewing nine window and data entry products for C. Complete field level functions specify prompt string, field length, data type, screen location, picture, target variable, entry rules, help messages, even functions to call for validation once data keyed in.

Windows for C is a subset. No data entry but all windowing functions. Unlimited windows can be made either to pop up or permanently overwrite the screen, scroll and highlight lists vertically and horizontally. Specify Compiler. Windows for Data: List **$295**, Ours **$259**. Windows for C: List **$195**, Ours **$149**.

BLAISE C TOOLS PLUS/5.0

C TOOLS PLUS/5.0 from Blaise Computing Inc. helps you to quickly build professional applications using the full power of Microsoft C 5.0 and QuickC. Now you can concentrate on program creativity by having full control over DOS, menus, interrupt service routines, memory resident programs, fast direct video access; windows; printer and keyboard control, and more!

Blaise Computing's attention to detail, like the use of full function prototyping, cleanly organized header files, and a comprehensive, fully-indexed manual, makes C TOOLS PLUS/5.0 the choice for experienced developers as well as newcomers to C.

C TOOLS PLUS/5.0 prebuilt libraries are ready to use with either QuickC or the Microsoft C 5.0 command line environment. Complete documented source code is included so that you can study and adapt it to your specific needs.

	List:	PC Express:
C TOOLS PLUS/5.0	**$129**	**$ 99**
Turbo C TOOLS	**$129**	**$ 99**
C ASYNCH MANAGER	**$175**	**$135**
Turbo POWER TOOLS	**$ 99**	**$ 75**
Turbo ASYNCH PLUS	**$ 99**	**$ 75**

PANEL PLUS

Library Source Code Gives It Complete Portability

There are no end of tools for screen design and data entry, but none quite like Panel Plus. Design a screen under program control, use Panel's utility to "run" and test it field by field, then pass it to Panel's code generator which delivers C source code. Options style the code to your compiler's liking, and you can of course do what you like to the source afterward. The code calls Panel Plus's function library, but now *the library comes in source,* so everything produced is highly portable. Not like other screen managers delivered as object libraries and which leave *you* to write the detailed code.

Panel Plus will operate in graphics mode via interfaces to graphics products it supports and can utilize the EGA's 43-line screen. Low-level I/O functions adapt it to various keyboards, screens, operating systems.

Panel's newest incarnation has every imaginable feature. A single screen design can have 1000 fields stacked as visual overlays up to 127 levels deep or as pop-ups. Groups of fields can be moved between levels. Screens can be output as compilable code or stored on disk for loading at run-time. Each field can be boxed, colored, multi-row, word-wrapped, and scrolled horizontally and vertically if larger than its on-screen view aperture. It can be assigned its own help and error message, can be told to accept certain characters, or to match a picture, and to check data after entry—proper dates, number ranges, etc.—using Panel's or your own validation routines. You can add your routines to Panel's test utility because even it comes as source. Fields are accessed in any order and control reverts to your application program after each field for choice of action.

For past Panelists, the new version has smaller and faster field and screen functions, tighter granularity, and an enhanced, reworked library. Major tool for the serious developer. List: **$495**, PC Express: **$395**.

POLYTRON VERSION CONTROL

Source Code Control for Any Language

PVCS allows programmers, project managers, librarians and system administrators to control the proliferation of revisions and versions of source code in software systems. Independent programmers, the leading software publishers and LAN companies, and hundreds of Fortune 1000 companies rely on PVCS to store and retrieve multiple revisions of text. It maintains a complete history of revisions as an "audit trail", generates status reports, and uses intelligent "difference detection" to minimize disk space for each new version.

On Corporate and Network PVCS simultaneous changes to a module are merged into a single new version. If changes conflict, the user is notified.

The "Logfiles" used to track changes are interchangeable between any PVCS product.

Corporate PVCS is for multiple programmers. It includes "branching" to maintain code when programs evolve on multiple paths. Personal PVCS offers most of the power and flexibility of corporate PVCS, but excludes multiple programmer features. Network PVCS is the Corporate version for LANs. File locking and security levels can be tailored to each project.

Ask for:	List	PC Brand:
Personal PVCS	**$149**	**$129**
Corporate PVCS	**$395**	**$329**
Network PVCS	**Call**	**Call**
PolyMake	**$149**	**$129**

C-WORTHY INTERFACE LIBRARY

The C-Worthy™ Interface Library wraps an entire user interface around your application. Its full power can be summoned by only a few high level calls. Sound exaggerated? A single function call can set up a complete text editor in a screen window. Recently acquired by Solution System, over 600 pages of Documentation, Turbo and Quick C version and a complete Interface Library have been added.

- High level calls pop menus and scrollable choice lists to the screen, restoring the background when dismissed.
- Windowing facilities open portholes of up to screen size for viewing virtual screens larger than the physical screen.
- Full context-sensitive help screen management takes over these chores and error messages. Automatic routines interrupt with pageable text windows explaining what to do next.

Novell found it "played a key role and accelerated development" in making its NetWare™ utilities easier for users. Ingenious demo: call for it.

Ask for:	List:	PC Express:
C-Worthy	**$195**	**$159**
with Forms Library	**$295**	**$269**

dBC *Identical dBASE III Plus Files Using C*

dBC™ is a series of C libraries from Lattice which creates, accesses and updates files identical to those of dBASE itself. So dBASE can read and update the files too.

What for? It means both C and dBASE applications can operate on the same data bases interchangably. It means C programmers can interface with the big market of dBASE users out there, yet side-step the dBASE language. It means dBASE applications can now be linked to the universe of C libraries and tools to add windows, graphics, statistical analysis, all the things dBASE cannot do. It means the speed and power of C to impress clients accustomed to dBASE!

dBC's functions parallel all dBASE's file handling commands, many decomposed to permit direct data manipulation. Our versions of dBC mimic file formats for dBASE II and III and now dBASE III Plus makes your programs network ready!... as many stations as a network allows. Hands-off mode handles record and file locking and unlocking automatically. Close in functions give you direct lock/unlock control.

Supports all four memory models. dBASE II, III...List: **$250**, Ours: **$175**. dBASE III Plus...List: **$750**, Ours: **$595**. Call for Source Code Pricing.

Payment: We honor MasterCard, Visa, American Express (no surcharge), checks in advance, or funds wired to PC Express, c/o Chemical Bank, 126 East 86 St., New York, Account 034-016058. COD (U.S. only) for cash, money order, certified check (no fee). NY State, add sales tax. Purchase orders accepted from larger corporations and institutions at our discretion if you agree to net 30 days plus 2% a month late penalty thereafter.

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THE SPINDRIFT LIBRARY

Fully Functional Fortran Library.

Spindrift's smooth package offers something previously unavailable to the Fortran buffs...a basket of functions, packed to the brim. No more tedious coding. Just call on Spindrift with it's armoury of functions.

Any number of Windows may be defined, each with a striking border and brilliant color. Define "pop-up" screens, Save/Restore images, set Cursor shape. Snare an entire screen into a Character array.

The Keyboard; read it without echo, or sense any keypress during execution. Cursor controlled directly with Edit keys.

DOS interface includes: Call System, Call Exec, Findfrst/Findnext for (*) and (?) file searching. Search the Path, subdirectory and file manipulation, command line argument parsing, date/time functions, DOS environment access, and much more. Other utilities also included.

Specify compiler, Microsoft or Ryan McFarland. List: **$149.00**. Us: **$129.00**.

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PC EXPRESS™ PROGRAMMER'S WORKBENCH

dBASE AT THE SPEED OF C

dBx Translates dBASE Applications to C

You dBASE™ programmers know what an expressive and readable language dBASE is. It's a very comfortable development environment. But the price is debased performance. Even compiled dBASE doesn't offer the speed that some users require these days. The kind of speed offered by software written in the C language. The answer is dBx™

dBx translates dBASE to C. It offers you a major competitive advantage over the next dBASE programmer: Keep writing in dBASE. Take every application all the way to completion. Then use dBx to translate them top to bottom to C!

Other advantages: C is portable, even to other operating systems like UNIX/Xenix™. To the Macintosh or Amiga. dBx gives your applications a passport to places dBASE cannot go.

Has its own file manager for single user, but links to major C file managers—c-tree and dBC—for compatibility with dBASE files or multi-user support. We have everything you'll need, including good advice.

	List:	Ours:
dBx	$550	$419
with Library Source	$950	$725

Call for Full Source Pricing

BRIEF/dBRIEF

The Power Environment for dBASE Programming

Many worthy utility products supply needs that dBASE®'s programming language doesn't—dUTIL™, dFLOW™ and a host of others. Trouble is, you have to use them separately, then combine their output into your dBASE program files.

No longer. dBRIEF™, written in BRIEF's macro language, grabs hold of BRIEF and turns it into a complete dBASE III and III Plus programming domain. Using BRIEF's underlying shell capabilities and its own interfaces, dBRIEF can run external utility libraries, plus dBASE itself, and link to the Clipper™, Foxbase+™ and Quicksilver compilers, all with dBRIEF still loaded and running the show. It can do what BRIEF already does plus:

- Convert a screen layout into dBASE code for interactive data entry.
- Display dBASE file structures in windows, a great convenience alongside your program files.
- Expand keystrokes into full dBASE statements.
- Indent automatically for clegic display.
- Create databases; index files; invoke Ashton-Tate's dFORMAT™ and dCONVERT™; draw lines and boxes.

"Simply marvelous programming environment for writing and editing dBASE programs.", *PC Magazine*, 7/86. Source code included!

Requires BRIEF 1.32 or later and 384k; 512k to run dBASE within dBRIEF; 640k and harddisk recommended.

BRIEF/dBRIEF...List **$275**,Ours: **$219**.

APPLICATIONS PLUS For dBASE

The Complete dBASE Companion

Who says you can't have it all?

APPLICATIONS PLUS has *everything* you need to get the most out of dBASE: An application generator (QUICKCODE PLUS), relational report writer (QUICKREPORT), and graphics system (dGRAPH).

QUICKCODE PLUS offers *dozens* of features you've *never* seen before in a dBASE code generator. Relational applications that read, display, and update a dozen or more databases simultaneously. "Real-time" calculations, performed *on screen* as the user enters each field. Forms up to 11 screens long, with the ability to pass data between screens. Computational formulas that automatically combine data from *different* databases. 9 Data types. 16 field types.

QUICKREPORT is a full-featured relational report writer, which combines up to 6 databases in one report, handles many-to-one relations, fancy printer features (like **bold** and *italics*), computed fields, and up to 16 levels of totalling and sorting.

dGRAPH is a graphics system that produces bar, pie, line, and piebar charts directly from dBASE data. Dozens of options let you tailor graphs to your needs.

APPLICATIONS PLUS is 100% compatible with Clipper and FoxBASE+.

	List:	Ours:
APPLICATIONS PLUS	$299	$249
QUICKCODE PLUS	$295	$170
QUICKREPORT	$295	$170
QUICKENTRY	$ 99	$ 59

MICROSOFT LANGUAGES

Powerful Implementations Of The Most Popular Programming Languages

Microsoft C 5.0: The flagship of the Microsoft line runs up to 30 percent faster than its predecessor. Its new optimization features deliver untouchable execution speeds, 100 new additional library routines...

Microsoft MacroASSEMBLER 5.0: If you ever wanted to take on the challenge of assembly, here's your opportunity. "MASM" 5.0 is a lot easier to use, has completely revised documentation, and a new "Mixed Language" programming guide that gives you step by step instructions for linking your assembly code with other Microsoft languages.

Microsoft QuickBASIC 4.0: is a revolutionary concept in BASIC programming. It allows you to run, edit, debug, and run again. Our friends at Microsoft have eliminated the dreaded compile step. Whenever you edit your code QB4 automatically incorporates your changes, so that it can run a program of 150,000 lines in less than a minute.

Each member of this language family includes the renowned debugger CODEVIEW.

	List:	Ours:
Microsoft C	$450	$295
Microsoft Macro-ASSEMBLER	$150	$109
Microsoft QuickBASIC	$ 99	$ 66
Microsoft FORTRAN	$450	$295

NOVELL: BTRIEVE, XQL, XTRIEVE

Sophisticated Tools Essential For Fast Database Handling

Btrieve is a library of subroutines that allows the programmer to build a database application using any language. It takes complete charge of all file creation, indexing, reading, writing, insertion, deletion, forward and backward searching. Its balanced tree indexing scheme finds any key in a million in less than 4 accesses...That's fast!

Btrieve is multi-lingual also. It includes more than 20 language interfaces (including C, BASIC, PASCAL, FORTRAN). However if it turns out that you are using something a little unusual, worry not. The manual includes a chapter on how to write a language interface to Btrieve.

Btrieve's vital statistics are equally impressive. Files may have up to 24 indexes; fixed record length to 4090 characters; variable length to 64K; indexes to 255 characters; files of 4 billion bytes. Network support includes Novell, 3-COM, IBM PC NET, Software Link's Multilink and many others.

XQL is a relational database management system designed especially for programmers. Imagine being able to access your database with the ease of SQL (Structured Query Language) statements and still having the power to process that data right down to the byte level.

Think about your applications. A large part of your software development effort is probably devoted to managing data stored in files on disk. Hours spent writing lines of code to search and store data records could have been used to program more important parts of your application. Why not let XQL do it for you. XQL will increase your programming productivity and let you focus on building better applications.

The XQL system works in tandem with Btrieve and has an equally powerful chassis...No limit on the number of records per file. Max. file size is 4 gigabytes, Max. record size equals 4K, Max. indexes per file is 24. The one version works for single or multiuser systems, DOS Ver 3.0 or greater. All languages are supported.

Xtrieve is the final ingredient in the Novell programming recipe. It is a menu driven, data retrieval system, that allows you to quickly find information and display reports. System developers can easily customize Xtrieve to display command menus, help files, and error messages in the English spoken by the customer. Xtrieve screens then gives menu choices that users can quickly recognize, making Xtrieve an easy product to use and understand.

Report Option for printing customized reports, form letters, mailing labels & statements.

	List:	Ours:
Btrieve	$245	$175
Btrieve/N	$595	$445
XQL	$795	$595
Xtrieve	$245	$220
Xtrieve/N	$595	$459
Report Option	$145	$128
Report Option/N	$345	$269

GSS GRAPHICS SYSTEM

Leave the Device Driving to GSS

For serious applications stick to the tools that stick to the standards. Not the least of reasons why GSS™ has emerged as the pre-eminent graphics toolmaker is that it has always conformed to ANSI standards.

At the heart of the system is the CGI standard Development Toolkit. It has all language interfaces and device drivers for keyboards, mice, joysticks, tablets, printers, plotters, cameras. The drivers completely insulate your application from concern for device idiosyncracy.

GSS Kernel™ conforms to ANSI's GKS 2b and has all its drivers and language bindings. Macro level tools to draw, color, segment, transform, store and recreate an object. The Metafile Interpreter reads ANSI CGM files with full CGI capability for recreation on various devices.

Quality software? IBM thinks so. They sell GSS under their own label. Royalties. Needs 256k.

	List:	Ours:
CGI Dvlpment Toolkit	$495	$425
Kernel System	$495	$425
Kernel for IBM RT	$795	$645
Metafile Interpreter	$295	$265

CLIPPER $399

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MORE PROGRAMMING TOOLS FOR...

dBASE, C, FORTRAN, BASIC, COBOL, PASCAL

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inference. The developer also must create a Report File for presenting object values to the client.

Run-Time Definition (RTD) files in Nexpert contain several different sections: Global; Start-Session; and Question, Menu, Property, Key, and End-Session Definitions. The Global Definitions section includes commands for which knowledge base to load and how to start the inference process (for example, automatically or in response to a function call).

The Start-Session Definitions option prompts the user to suggest hypotheses and volunteer information before inferencing begins, while the End-Session Definitions option directs the system to display reports after inferencing. Unfortunately, Nexpert includes no tools to help build these files from scratch, and the developer bears responsibility for learning how to use the language creatively.

The developer composes Report Files using yet another formatting language, which includes statements to control text positioning, attributes, and conditionals on object values. After constructing the RTD files, the developer can run the application under NORT by executing Nexpert with the name of the RTD file.

NORT's application-delivery environment has a number of advantages over competitors, including the capability to create custom-designed screens, the ability to control the environment with a programming language, and the option to use a text editor. Another useful feature is the ability to specify generic forms for classes, objects, and properties. The RTD file specifies use of a particular form whenever a property value of an object in zero or more specified classes is sought. Many of the other low- or midrange expert systems lack this capability.

NORT also makes it easy to specify questions and forms for specific hypotheses and to assign functions to key combinations at runtime. NORT provides an additional way to display text and graphics files directly by including commands in the RTD file. At present, however, NORT supports graphics created and displayed only on an EGA system. After the RTD file completes the inference process, control returns by default to the NORT main menu.

Like other Nexpert features, NORT is too complex for beginners. Although NORT has a menu-based development interface, it shares some similarity and terminology with the Nexpert development screens and can be confusing.

POWERFUL POSSIBILITIES

Several excellent features help Nexpert Object stand out as a powerful, innovative development toolkit for practical applications. Integration of backward-

NEXPERT'S RECENT UPDATE

Neuron Data recently announced version 1.1 of Nexpert Object. According to the company, new features include a stricter syntax and enhanced syntax checker, a compiled format for saving knowledge bases, string and date conversion functions, categories on rules and slots to dynamically disable forward and backward chaining, enhanced facilities for object and rule editing (including flip pages), and integer, date, and time data types. The product's documentation, a major problem with version 1.0, has been dramatically improved.

In addition, Neuron Data has added new debugging capabilities and design aids, such as breakpoints, session journaling, and a view line that displays a complete string when browsing the rule network. The Callable Interface now has calls to compile a knowledge base or structures, control journaling, and change inference strategy.

The company announced two add-on tools. NEXTRA, a Macintosh-based knowledge-acquisition tool, obtains information from the user through interactive interviews, structures the knowledge into logical relationships, graphically represents the knowledge, and automatically generates rules and objects. NEXTRA applications can be imported into Nexpert applications running on other platforms. V.I. Corporation is developing another Nexpert add-on product—a bridge to link DataView with Nexpert to provide interactive and dynamic graphics capabilities similar to those found in Texas Instrument's Personal Consultant Plus.

—Maxine Fontana

and forward-chaining mechanisms with dynamic control over the process allows the developer to customize the inference process to an extraordinarily detailed level. The sophistication of resulting systems is limited only by the developer's ability to track and debug the process—which is greatly aided by the Inspector utility.

The symmetry of Nexpert rules is an elegant approach, making possible powerful inference behavior. In addition to inheriting properties from multiple ancestors (which sets the frame-structuring capabilities apart from most low- and midrange tools), Nexpert objects and classes also can inherit properties from multiple descendants, making true frame lattices possible.

Nexpert's original documentation is, unfortunately, the system's worst feature. A developer has no choice but to wade through pages of background material on expert systems and AI that is so poorly presented that users will become mired in confusion over even elementary concepts. As this article was being prepared, however, Neutron Data announced version 1.1 of Nexpert Object. In the new version, the company has addressed many of the deficiencies in the documentation and has added new features and capabilities (see the accompanying sidebar.)

Nexpert is an excellent set of tools for a wide range of application requirements and developer skills. It offers developers well-versed in traditional languages, such as C, an extremely powerful environment for developing expert systems. Moreover, the ability to embed Nexpert in other types of software sets it apart from other shells and gives it a tremendous base of potential applications—made all the more inviting to prospective developers by the elimination of a direct user interface. Systems produced this way can be more complex, more sophisticated in their information needs, and better streamlined for specific application environments. Nexpert is a powerful tool that heralds the arrival of a new wave of integrated expert systems.

Neuron Data
444 High Street
Palo Alto, CA 94301
415/321-4488
Nexpert Object: $5,000

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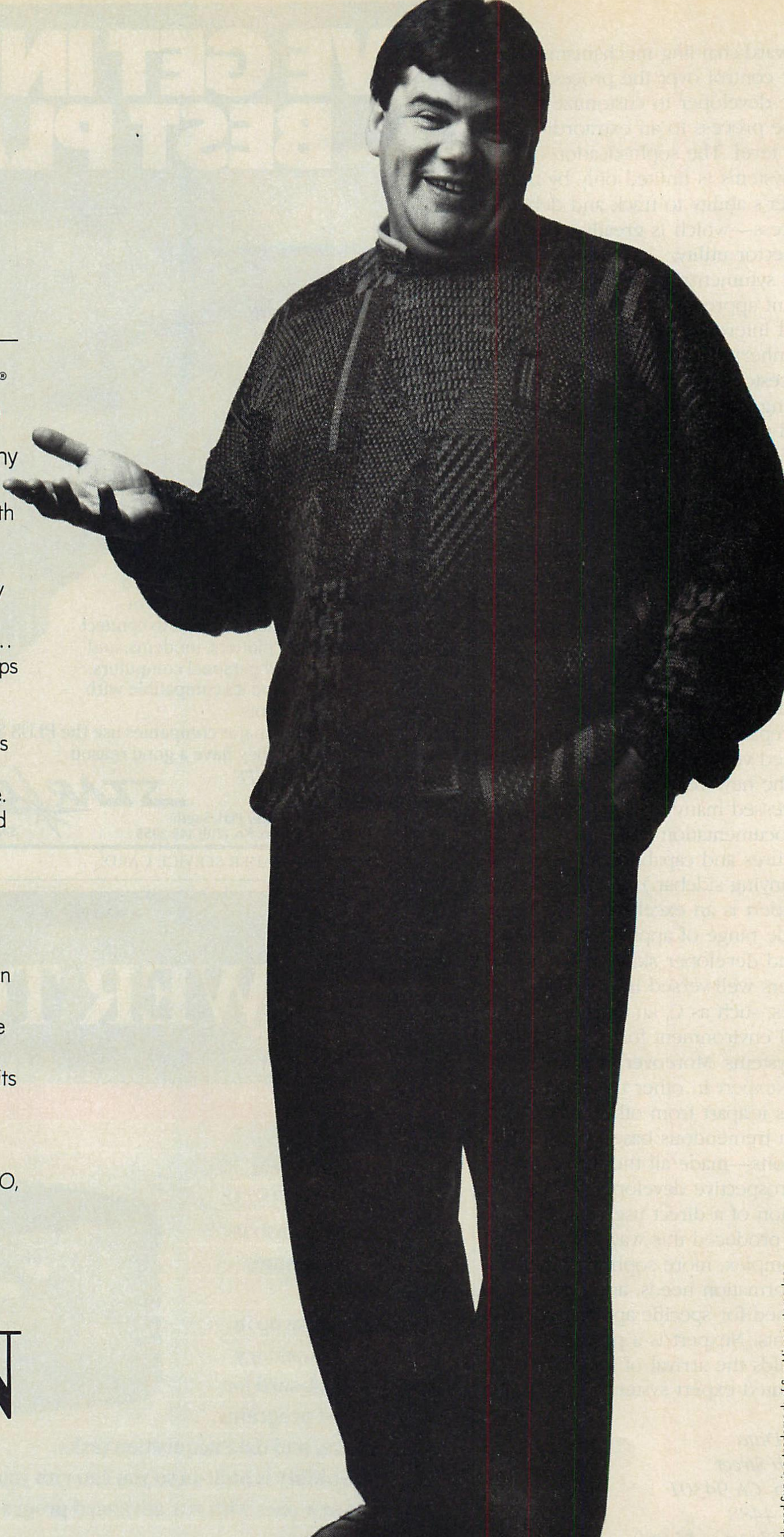
Tom Arcidiacono is an instructor of computer science at the New York Institute of Technology and a consultant in knowledge-based systems development.



PRODUCT WATCH

Reviews and Updates

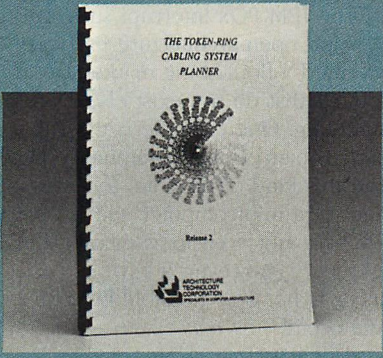
TOKEN-RING CABLING SYSTEM PLANNER 2.0
Architecture Technology Corporation

KEYWORKS ADVANCED VERSION 1.0
Alpha Software

TOKEN-RING CABLING SYSTEM PLANNER 2.0

Architecture Technology Corporation
P.O. Box 24344
Minneapolis, MN 55424
612/935-2035

PRICE: $295



CIRCLE 335 ON READER SERVICE CARD

Building a LAN is not a task to be taken lightly—particularly the planning stage. Whether the project involves five PCs or a multi-LAN system, the network designer should develop a comprehensive plan before the installer pulls the first cable.

The Token-Ring Cabling System Planner 2.0, from Architecture Technology Corporation, helps the network designer do just that. The database program keeps track of all IBM Token-Ring cabling specifications, determines costs, and checks for Token-Ring design-criteria violations.

The plan for a network, called a layout, can include a work group, a floor of a building, a department, or multiple Token Rings. The designer can combine as many as 40 layouts to create one large master layout.

The program's main menu has four options: main, reports, database, and miscellaneous. Navigating the program with familiar pull-down menus is reasonably intuitive, but a careful review of the manual is recommended to insure understanding of the terminology and requested information.

The database option assigns costs to component names. The cost database option calculates the cost of the total network installation, including component costs, labor rates, and per-foot charges for cable. The miscellaneous menu allows the designer to turn the screen color on or off; duplicate, rename, or erase files; switch to a new directory; or check memory status.

The designer enters information with a moving viewport (representing an area of 20-by-74 feet). One screen character equals 1 foot, and virtual floor space can be a maximum of 1,000-by-1,000 feet (grid coordinates 0 to 999). The designer moves around the virtual screen using the Tab and cursor keys or with a mouse (by using the /m option to invoke the program from the command line). Cursor movement is quick because the planner uses character-mode video.

An office floor plan with a transparent grid overlay and a sketch of the network helps locate exact coordinates and resolve design errors. The designer enters information for a component by moving to the desired grid coordinates and entering the first letter of the device (an F, for example, to locate a faceplate, or a W for a wiring closet). The designer can place several components at the same grid coordinates with the wiring-closet descriptor, including faceplates, multistation access units (MAU), panels, repeaters, and surge suppressors.

Information required for each network item includes cable type and ID, ring number, source and destination location, and distance calculation method. The program automatically calculates direct line or right-angle distances once the two ends of a cable are identified, or the designer can calculate and enter the distances and extend the calculated cable distances to account for nonstandard ceiling heights or use the default setting of 20 feet.

Faceplates require additional information that includes faceplate type, adapter address, and device ID, such as "Joe's AT" or a number scheme. Components other than faceplates require a description in addition to the data items mentioned.

The program defines all cable runs from the workstation to the wiring closet and back to the workstation. When it encounters a second occurrence of a cable ID, the program copies the database information into the current layout and completes the distance calculations. It is best to key either all the workstation information first or all the wiring closets first.

The designer edits components on the layout by placing the cursor over the letter representation and pressing the Enter key. A window pops up with the following options: show/edit, to look at or change the component information; move, to move the component to another grid location; trace, to show a highlighted trace of where (but not how) the cable runs; and delete, to delete the component from the layout. The slash key accesses the global menu within the layout.

Once all of the unit-cost, cabling, and component information is complete, the designer can generate character-based reports printed on 8.5-by-11-inch paper. The cable-list report catalogs all cables in a specified group of layouts, with options to sort by cable ID, component description, or source location. Most cables will have two entries, one for source and one for destination; single-entry cables are exceptions and need to be investigated or explained. The estimated cost report applies the cost database to the list of components and cable lengths and generates a total cost for the network. An ID-labels report generates cable labels.

The locator-chart feature is similar to IBM's locator chart and supplies the Token-Ring adapter information for the network with the appropriate 48-bit address, device ID (usually a PC name), ring number, and MAU ID. The ring-sequence chart lists the main ring path connecting each MAU to another MAU and is an automated version of IBM's ring-sequence chart.

The summary report gives a list of all components, cable runs, and lengths and calculates total cable lengths, adjusting for different cable types (the baseline is cable types 1 and 2 as in the IBM documentation). The report also estimates the approximate propagation delay in the main ring and in the total ring when all devices are active. The exception report, usually associated with a planning piece of software, shows all violations of documented Token-Ring design criteria.

The program did a good job of catching open-ring errors and excessive lobe lengths in a layout intentionally created with several design-constraint violations. The program also issued a warning about using type 6 (patch cables) longer than 150 feet.

The planner failed to supply a correct error message, however, when the adjusted ring length (ARL) combined with the longest lobe exceeded the maximum design allowance. With an ARL of 1,539 feet, the planner stated, "Warning: 47 feet exceeds the recommended maximum lobe length of −419." A clearer error message could have been, "Warning: the ARL exceeds maximum design distances."

The planner also failed to reset the error messages in the database when a component was moved on the layout from an error location to a valid location. The user must enter a new component in the layout to reset the error message. Architecture Technology plans to fix these bugs in a future revision.

Overall, the Token-Ring Cabling System Planner is a useful tool that can expedite some of the less desirable chores necessary to plan a network. The product, however, is not a replacement for careful planning. Moreover, because the planner lacks a detailed discussion of Token-Ring design constraints, it is best suited for the network designer who is already familiar with Token-Ring concepts. The experienced designer building small departmental networks that eventually expand into larger LANs will find this program particularly worthwhile.

—GARY GUNNERSON

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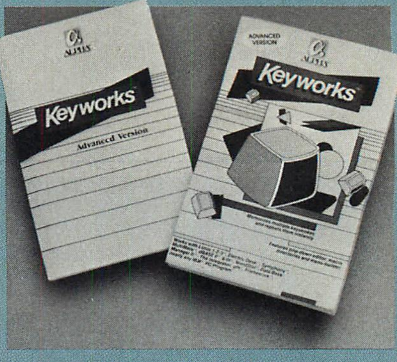

CIRCLE 336 ON READER SERVICE CARD

The IBM PC's interrupt structure and open architecture have created a flourishing market for products that do not exist elsewhere in computing. One example is the keyboard enhancer. A programmer cannot write this kind of program for a mainframe or a minicomputer with an ASCII terminal—not even in assembler. On a desktop PC, however, a keyboard enhancer is not only possible but often quite useful.

Alpha Software Corporation's Keyworks Advanced Version 1.0 is a keyboard-enhancer program of the genre pioneered and dominated by RoseSoft's ProKey (the first successful keyboard enhancer) and Borland's SuperKey. Keyworks has some additional features that will be of particular interest to microcomputer managers, dealers, and VARs.

Similar to ProKey and SuperKey, Keyworks is loaded into memory after bootup and remains resident. It steals the PC's keyboard-interrupt vectors and gets an opportunity to intercept keyboard signals before anything else, including MS-DOS. This allows the user to redefine any key on the keyboard as any combination of keys. The F1 key, for example, could be redefined to send the codes for "dir /w" instead of its usual code.

These convenient macros also can substitute for lengthy keystrokes. Lotus 1-2-3 or word-processor users, for example, can place a frequently executed sequence of commands into a macro and press a single Ctrl- or Alt-key combination instead.

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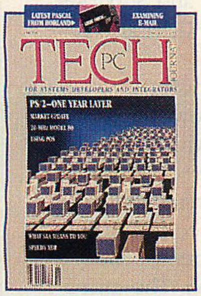

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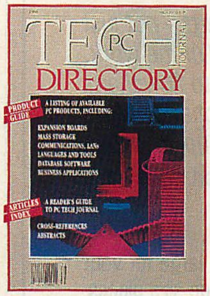

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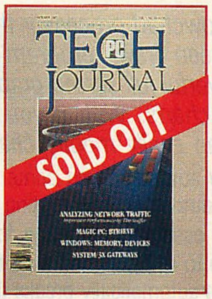

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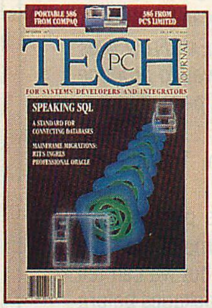

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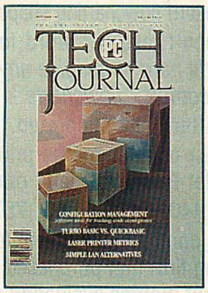

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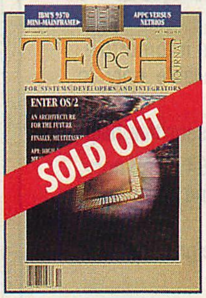

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In addition, Keyworks permits another kind of redefinition. Besides defining single keys, the user can define the sequence "asap," for example, to be shorthand for the words "as soon as possible," allowing the user to define text for memos, forms, and program source code within a word processor or text editor. ProKey and SuperKey (when used with SideKick) also have these functions.

What sets Keyworks apart from the other two products, however, is its programming language, which permits macros to incorporate sophisticated logic. Its macros can read and write to the screen, check to see if specific text is displayed, display menus, and prompt for information. The micro manager can use Keyworks to inexpensively integrate disparate programs without buying into an environment such as Quarterdeck's DESQview or Microsoft Windows. Keyworks is available in a Standard Version and an Advanced Version. Only the latter has this programming language.

To install Keyworks, the user simply copies the diskette to an appropriate directory. A setup program is provided, but is needed only if the user wants to change the default values for the macro and text buffers, key assignments, or the program's window border and screen colors. After installation, KEYWORKS.EXE must be called from the AUTOEXEC.BAT file to install the program each time the PC is booted.

The user activates Keyworks by pressing the plus key on the numeric keypad (called the menu key, it can be reassigned if needed) and a small menu is displayed in the upper left-hand corner of the screen. A reassignable bypass key tells Keyworks not to process the next key as a macro.

A host of control functions are available from the menu. Otherwise, Keyworks silently monitors the PC's keyboard, checking for macros and shorthand. To define a macro, the user must pop up the menu and tell Keyworks to record keystrokes until the definition is complete. Once saved, the user can edit the keystrokes in source-code form. The source code for Keyworks macros resembles Lotus 1-2-3 macros. Key words and special keys are enclosed in braces. Other main-menu options include a DOS file manager, file encryption and decryption, and a cut-and-paste function.

Although developers actually program with Keyworks, Nicklaus Wirth can rest easy: the Keyworks macro lan-

guage will never replace Pascal as a structured language for writing complex applications. For a macro processor, however, the Keyworks macro language is powerful; it includes statements for text I/O, matching text on the screen, arrays, looping, conditionals, logical operations, labels, and invocations of macros as subroutines. Macros can even be placed on disk and loaded from other macros as needed, permitting the developer to write large applications.

Keyworks has a 10,000-keystroke macro buffer, but screen I/Os and menus can quickly fill this up. External macros, which the developer can create through the main menu, solve this problem. The main menu parses a normal macro and stores it in a file with the macro ID as the name and .KBI as the extension. By referencing the macro name, the developer can call an external macro from a RAM-resident macro. An external macro cannot call another external macro, but a clever programmer can circumvent this with a driver macro and control variables. A developer can create many external macros because each is a separate file.

The programming language also includes powerful screen operations, such as positioning the cursor, displaying text and menus (including the Lotus moving-bar type), prompting for information, drawing boxes, and saving and restoring the screen. Keyworks also provides slides, which are captured screens (text only, unfortunately) that the user can redisplay and use for a demo program or a help system within an application.

Keyworks supports print-enhancement macros, which are macro strings directed to the printer (serial or parallel), but not to the screen and keyboard. Print macros are prefixed with an ampersand and followed by a single character. The user embeds them in on-screen text (such as spreadsheet text cells). When the spreadsheet is printed, Keyworks intercepts the ampersand, looks up the macro, and inserts the appropriate control strings. This capability allows effective use of laser printers, which allow multiple fonts, different type sizes, and special effects from programs that do not normally support these printer features.

If Keyworks has a weakness, it is macro debugging—only a simple, single-step facility is included, which makes entering and testing complex macros tedious. Writing a Keyworks macro is actually programming; despite the unusual environment, the rules of good programming still apply—proper design and structure, followed by thorough testing of code.

Having to program macros is a small price to pay for the power Keyworks provides. Its macro language suggests many unusual applications. A product developer could write macros that allow an untrained salesperson to demo software with one key, complete with annotated screens. A help system could be added to a complex program, complete with local operating procedures. An accounting package could be streamlined with additional macros and print enhancements.

Considering the cost of moving these applications to Windows or DESQview (for older, larger, or less friendly programs, this is not even an option), Keyworks is a cost-effective integration tool. Dealers, VARs, and microcomputer support managers should give this product a close look.

—MARTY FRANZ

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CIRCLE NO. 162 ON READER SERVICE CARD

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1 1,280-BY-480

This month's item is a demonstration of how to extend the capabilities of the VGA into uncharted territory, effectively doubling the number of pixels available on a standard VGA screen. For text displays, the methods presented here offer the potential for displaying almost five times the number of characters shown in the standard 80 columns by 25 rows, which would be well appreciated by users who measure their spreadsheets by the acre. Most applications deal only with a limited set of screen dimensions; as a result, this method is not meant for retrofitting to existing programs, but is offered to developers for incorporation into future applications.

This item was submitted by Arun Johary, Technical Marketing Engineer, and Bo Ericsson, Graphics Software Engineer, both of Chips & Technologies Inc. in San Jose, California.

1 DOUBLING EFFECTIVE VGA RESOLUTION

The standard VGA supports a maximum resolution of 640-by-480 pixels in graphics modes. When displaying characters, the pixels can be collected into character cells in various ways, yielding a different number of rows and columns depending on the pixel dimensions of each character. With the standard fonts built into the VGA ROM, a graphics screen can display either 80 columns by 30 rows, using an 8-by-16 pixel font, or 80 columns by 60 rows, using an 8-by-8 pixel font. Other combinations can be obtained by directly programming the video registers, provided that a font in a suitably sized character box is available.

For example, a four-pixel-wide font allows the display of 160 characters on each line. Characters created with a four-pixel font, however, are hardly readable and are not suitable for long-term viewing. Under normal circumstances, a user prefers to look at a larger font that presents less information but has better visibility. On occasion, however, it is useful to zoom out and see much more information on the screen—for example, the overall layout of a spreadsheet or the formatting of a wide document.

Many EGA and VGA adapters include video drivers that establish high-density text modes for a variety of applications. Switching in and out of these modes, however, usually requires exiting and then restarting the application. Ideally, switching screen modes should be possible from within applications; it should be instantaneous, and it should not require the entire screen to be redrawn. The hardware features of the VGA allow a programmer to implement a scheme such as this.

The VGAZOOM program (portions of which are printed in listing 1) puts the VGA into a high-resolution display mode that displays text in 160 columns by 60 rows. At the touch of a key, the display switches into a low-resolution mode of 80 columns by 60 rows, maintaining the contents of the video buffer and continuing to display the left half of the screen. The user can then scroll left and right to display any portion of the 160 columns, or press a hot key to restore the high-resolution display.

To counterbalance the poor readability of a four-bit font, the 160-column mode is implemented by configuring the VGA to simulate a monochrome bit map of 1,280-by-480 pixels. Text is then written to this bit map with the VGA's built-in 8-by-8 pixel font. Although a text application is described, the hardware is actually in a bit-mapped, all-points-addressable graphics mode. A similar technique can be used to display graphics at almost twice the standard VGA resolution.

The high-resolution mode is obtained by programming the VGA to display a single pixel on the screen for every two pixels in video memory. Thus, a scan line with 640 pixels across the screen holds the information from 1,280 pixels in memory. Combining pixels in this way, however, loses information; the four possible values of a pair of pixels are reduced to only two possibilities in a single pixel.

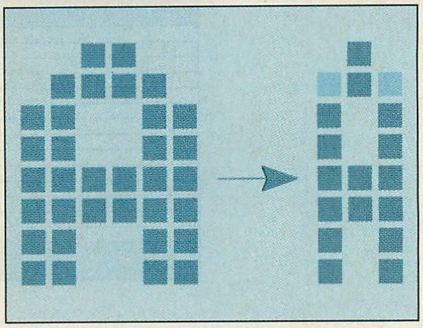
The loss of information introduces distortion, known as *aliasing*, into the displayed image. The characteristics of the VGA monitor, however, allow applying an antialiasing method to recover some of this lost information, thereby improving the appearance of the four-bit font.

Antialiasing, a technique in which color resolution compensates for lack of spatial resolution, is used extensively in commercial television broadcasts. A television set has very low spatial resolution, but can display virtually unlimited variations of colors and shades. The many colors compensate for the few pixels, resulting in an image that is very satisfactory to the eye. In most cases, the quality of the image appears to be higher on a standard television screen than on a high-resolution computer monitor.

Because it is an analog device, a VGA monitor also can display a large number of shades. A single pixel need not simply be on or off, but can be displayed in a variety of shades. In the case at hand, the pixel in the four-bit font is displayed in one of three gray levels depending on whether its two constituent pixels are both on, both off, or one on and one off. In a graphics application, a fourth level can be obtained by distinguishing between the on-off and off-on cases, but this yields no benefits in displaying text.

This technique, illustrated in figure 1, results in characters that, if still not suitable for full-time viewing, are quite readable over short periods of time. The appearance could be improved by designing an eight-bit font specifically

FIGURE 1: *Compression*



Two pixels of the image in video memory (left) are combined to produce one pixel on screen (right). Antialiasing uses different shades to represent diagonals and horizontals.

for compression and antialiasing, but even the standard built-in font gives acceptable results.

Implementing VGAZOOM requires the reprogramming of four major VGA characteristics. A comprehensive explanation of register-level VGA programming is not appropriate here, but this description assumes that you are familiar with the VGA architecture as described in IBM's *PS/2 Hardware Interface Technical Reference*.

The first consideration is the mapping of display memory in the CPU address space. In a 16-color graphics mode, each byte written by the CPU to the video buffer is expanded by the VGA hardware to four bytes, one byte in each of the four bit planes. In the monochrome modes that are used in VGAZOOM, each byte of display memory maps to one byte in the CPU address space, so that each bit in memory represents one pixel. The video memory mapping is controlled by the contents of the memory-mode register at offset 4 of the sequencer register set.

The second characteristic is the mapping of video memory to the screen via the shift registers. To display the contents of the video buffer, the hardware loads a 32-bit word from the buffer into the shift registers. At each cycle of the dot clock, one, two, or four bits are shifted out of the registers into the dot generator, creating one pixel on the screen.

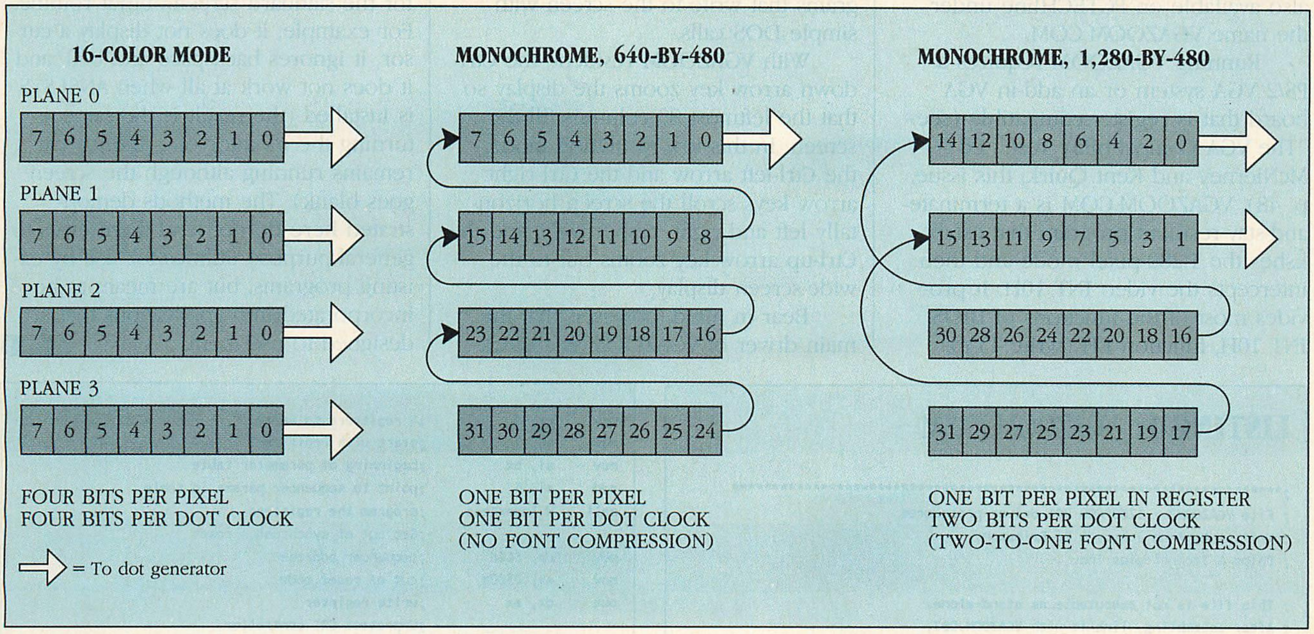
Figure 2 shows three different VGA modes. In 16-color mode, the registers are programmed to send four bits per clock. The registers are shifted out and must be reloaded for every eight cycles of the dot clock (one cycle of the character clock).

In monochrome mode, the 32 bits in the shift registers represent 32 pixels. To generate 640 dots per scan line, the shift registers are chained together and produce one output bit per dot clock, emptying the registers in 32 clocks. To simulate 1,280 dots per scan line, the shift registers are programmed to produce two output bits per dot clock. These two bits represent two pixels in video memory but produce one pixel on screen, resulting in the 2:1 font compression described previously. In this case, the shift registers must be reloaded every 16 dot clocks.

Programming the shift registers requires writing to three VGA registers. The graphics-mode register, offset 5 of the graphics-controller register set, controls the chaining of the registers into 1, 2, or 4 parallel units. The color-plane-enable register, offset 12H of the attribute-controller register set, controls how many bits are sent to the dot generator at each clock cycle. Finally, the clocking-mode register, offset 1 of the sequencer register set, determines the frequency of reloading the shift registers—every 8, 16, or 32 dot clocks.

The third programming consideration is the establishing of a gray scale that implements the antialiasing

FIGURE 2: *Video Shift Registers*



The configuration of the shift registers and the number of bits fed to the dot generator control the mapping of bits from the video buffer to pixels on the screen. For the standard 640-by-480 16-color mode, BIOS establishes the left configuration. The VGAZOOM program uses the middle configuration for the 640-by-480 mode and the rightmost one for the 1,280-by-480 mode.

scheme. The final color of a pixel is determined in the digital-to-analog converter (DAC) that produces the analog signals for the display. The DAC contains 256 color registers, each 18 bits wide, allowing the display of 256 simultaneous colors from a palette of 262,144 colors. When a pixel is processed by the dot generator, the value of the bits that make up the pixel is used to select one of these color registers, and the contents of the register are used to establish the levels of the red, green, and blue video signals that the DAC sends to the display. In the 1,280-pixel mode, the two bits representing each on-screen pixel can select one of the first four color registers. They are loaded with values representing black, gray, gray, and white, corresponding to both bits off, one on, one off, and both on, respectively.

The final consideration is fine-tuning the parameters in the CRT controller registers to produce the best-looking display in each mode. These values are best determined by experimentation; the values used in the accompanying program work well on IBM PS/2 systems.

Listing 1, VGAZOOM2.ASM, shows the major procedures that establish and use the 1,280-pixel graphics mode.

SetMode initializes the VGA to either the 1,280- or 640-pixel mode by writing appropriate values to all of the VGA registers. The two tables defined in the procedure contain the parameters for each mode. Comments in each table give its general content. To demonstrate exactly how much antialiasing improves the display in 1,280-pixel mode, compile and run the program after setting the palette data in HTABLE to the same values as in LTABLE. This removes gray-scaling, discarding half of the information content of the 8-bit font; the result is hardly readable.

W_Palette sets up the external palette in the DAC. The inputs to the procedure are the I/O address for the address register, the index of the first palette register, the number of palette registers to be written, and a pointer to a memory table of color values. Loading a color register involves four steps: writing the index of the target register to the address register and then writing three bytes of red, green, and blue color values (in that order) to the next sequential I/O address. The hardware concatenates the six low-order bits of each byte to form the 18-bit palette value and then automatically increments the index in the address register. Therefore, loading a sequential set of registers requires sending one index of the first register and then successive triplets of color values.

Another procedure, Drawchr, draws a character on the screen. The inputs to the procedure are the address in the display memory to receive the character, the base address of the font table, the ASCII-character code, and the character height in scan lines. The procedure assumes a fixed font width of 8 pixels. Note that even in 1,280-pixel mode, the software writes characters to video memory in an 8-bit font; it is the hardware that performs the compression to the 4-bit font as the characters are displayed.

Vert_Scroll scrolls the display either up or down. The inputs are the font width and the number of lines to scroll up (a negative number means the number of lines to scroll down).

The procedure Horiz_Scroll_4 scrolls the display left or right in 640-pixel mode, using the VGA hardware scrolling capabilities. The inputs are the bit-map width and the number of pixels to scroll right (a negative number means scroll left). Rd_IndexReg, W_Index_Regs, and W_Attr_Regs are utility routines that simplify the tasks of reading from and writing to the various VGA registers.

The routines in the listing are not executable as printed because they lack a main program. A demonstration program that uses them, VGAZOOM, is too large to print here but is available on PCTECHline (along with VGAZOOM2). To build the program, assemble both VGAZOOM and VGAZOOM2, link the two object files together, and convert

the program to .COM format with EXE2BIN. This executable version is also available on PCTECHline under the name VGAZOOM.COM.

Running VGAZOOM requires a PS/2 VGA system or an add-in VGA board that is register-compatible (see "The VGA Compatibility Test," Ed McNierney and Kent Quirk, this issue, p. 48). VGAZOOM.COM is a terminate-and-stay-resident program that establishes the 1,280-pixel mode and then intercepts the video INT 10H. It provides most of the functions of BIOS INT 10H, function EH (write TTY); therefore, it can display the output of COMMAND.COM and most other programs that write to the screen with simple DOS calls.

With VGAZOOM resident, the Ctrl-down arrow key zooms the display so that the leftmost 80 columns fill the screen. In this low-resolution mode, the Ctrl-left arrow and the Ctrl-right arrow keys scroll the screen horizontally left and right, respectively, and the Ctrl-up arrow key zooms out to the wide-screen display.

Bear in mind, however, that the main driver of VGAZOOM is a quick-and-dirty demonstration program; it is not meant as a permanent replacement for the standard screen-output routine. For example, it does not display a cursor, it ignores backspace and bell, and it does not work at all when ANSI.SYS is installed (the result is the same as turning the monitor off—the system remains running although the screen goes blank). The methods demonstrated here do not lend themselves to general-purpose utilities for use by existing programs, but are meant to be incorporated into applications that are designed to use them.

LISTING 1: VGAZOOM2.ASM

```
;***********************************************************************
; File VGAZOOM2 - 1280*400 VGA driver procedures
; Written by Arun Johary & Bo Ericsson,
; Chips & Technologies Inc.

; This file is not executable as stand-alone.
; After assembling, link it with VGAZOOM.OBJ,
; then convert to .COM with EXE2BIN.

; Resulting VGAZOOM.COM is a TSR for implementing 1280x480 mode,
; with zooming to/from 640X480 mode and panning.
;***********************************************************************

LORES equ 0
HIRES equ 1

public DRAWCHR
public SETMODE
public HORIZ_SCROLL_4
public VERT_SCROLL
public EndOfProgram

code segment para public 'code'
     assume cs:code

;***********************************************************************
SETMODE proc near
; This procedure programs the VGA registers for one of two
; modes depending on AX
;  AX  = HIRES -- high resolution 1280*400 monochrome mode
;  AX  = LORES -- 640*400 monochrome mode

        push    cs       ; DS = CS because parameter tables
        pop     ds       ;  are in the current segment
        cld              ; clear for subsequent auto increment
        cmp     ax, HIRES       ; Hires mode ?
        jne     SetMode01       ; if no, test for LORES mode
        lea     bx, HTABLE      ;HIRES table selected
        jmp     SetTheMode      ;program the parameters
SetMode01:                      ;Test for LORES mode
        cmp     ax, LORES       ;LORES mode ?
        jne     SetMode_End1    ;invalid parameter, return to caller
        lea     bx, LTABLE      ;lores table selected
        jmp     SetTheMode      ;program the parameters
SetMode_End1:
        jmp     SetMode_End
SetTheMode:                     ;Sync reset while programming mode
        mov     dx, 3C4H        ;sequencer address
        mov     ax, 0200h       ;sync. reset
        out     dx, ax          ;write the register
                                ;Set miscellaneous output register
        mov     dx, 3C2H        ;miscllaneous output register address
        mov     al, [bx+9]      ;table value for Misc Output Register.
        out     dx, al          ;write the register
                                ;Set sequencer registers 01-04
        mov     dx, 3C4H        ;sequencer address
        mov     cx, 4           ;4 registers to write
        mov     ah, 1           ;start with register 1
        mov     si, bx          ;beginning of parameter table
        add     si, 5           ;point to sequencer params in table
        call    W_IndexRegs     ;program the registers
                                ;Get out of synchronous reset
        mov     dx, 3C4H        ;sequencer address
        mov     ax, 0300h       ;out of reset mode
        out     dx, ax          ;write register
                                ;Unprotect CRT controller
        mov     dx, 3D4H        ;crtc address
        mov     ax, 011h        ;vertical sync end register
        out     dx, ax          ;set protect bit (D7) to 0
                                ;Set CRT controller registers 00-18
        mov     cx, 25          ;25 registers to write
        xor     ah, ah          ;start with CRTC register 0
        mov     si, bx          ;beginning of parameter table
        add     si, 10          ;point to CRTC parameters in the table
        call    W_IndexRegs     ;program the registers
                                ;Set Graphics controller regs 00-08
        mov     dx, 3CEH        ;graphics ctrl address
        mov     cx, 9           ;9 registers to write
        xor     ah, ah          ;start with GC register 0
        mov     si, bx          ;beginning of parameter table
        add     si, 55          ;point to GC parameter in the table
        call    W_IndexRegs     ;program the registers
                                ;Set Attribute controller regs 00-14
        mov     dx, 3DAH        ;Status register address
        in      al, dx          ;reset attribute flip-flop
        mov     dx, 3c0h        ;attribute ctrl address
        mov     cx, 20          ;20 registers to write
        xor     ah, ah          ;start with register 0
        mov     si, bx          ;beginning of parameter table
        add     si, 35          ;point to Attr. Ctrl params in table
        call    W_Attr_Regs     ;program the registers
        mov     al, 14h         ;write to Attribute color select reg
        out     dx, al          ;(not stored in parameter table)
        xor     al, al          ;data = 0
        out     dx, al          ;write data
        mov     al, 20h         ;reenable video
        out     dx, al          ;write the index reg to reenable video
                                ;Set external palette
        mov     dx, 3C6H        ;Palette mask register
        mov     al, 0ffh        ;enable all 8 bits
        out     dx, al          ;write the mask
        mov     dx, 3C8H        ;Palette address register
        lea     si,[bx+64]      ;point to palette parms in table
        xor     ah,ah           ;start at palette reg 0
        mov     cx,4            ;set 4 colors
        call    W_Palette       ;program the palette registers
SetMode_End:    ;end of this procedure
        ret

;***********************************************************************
; These two tables provide parameters for programming VGA hardware
; in each of two modes.

;***********************************************************************
HTABLE label byte  ; parameter table for 1280*400 mono mode
```

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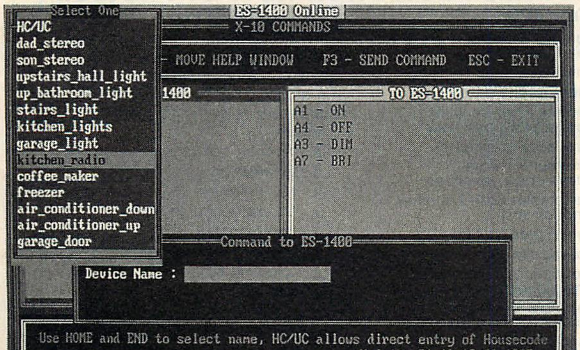

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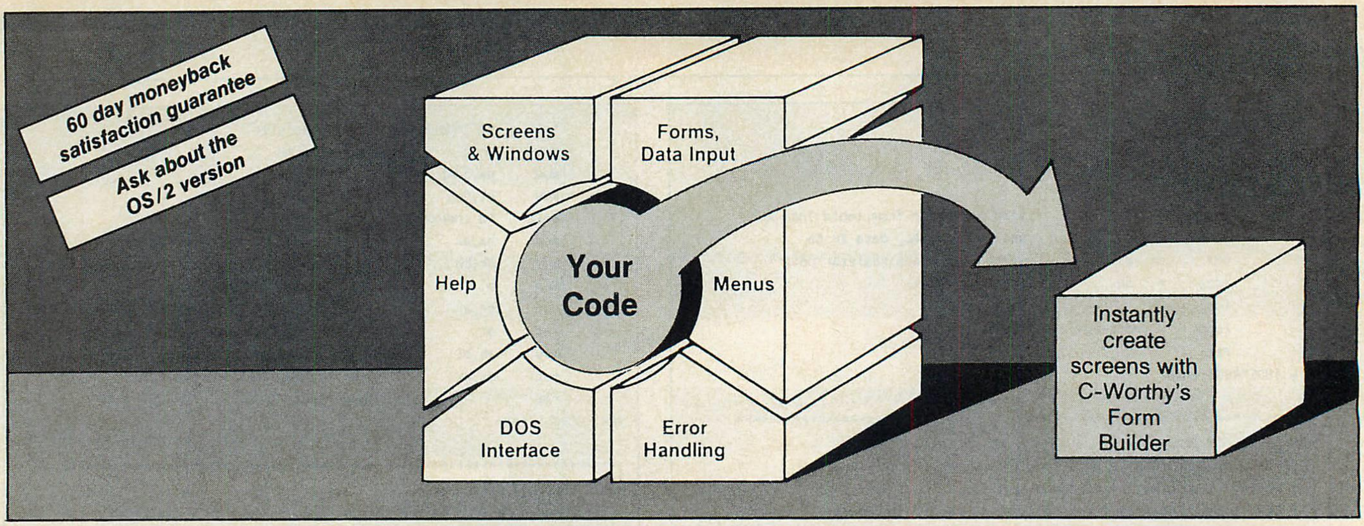
```
db 000h, 000h, 000h, 000h, 000h    ; Dymmy header
db 005h, 00Fh, 000h, 00eh          ; Sequencer offsets 01-04
db 063h                            ; Miscellaneous register

                 ; CRT Controller offsets 00-18h
db 05Fh, 04Fh, 050h, 082h, 054h, 080h, 0bFh, 01Fh
db 020h, 000h, 000h, 000h, 000h, 000h, 000h, 000h
db 09ch, 00eh, 08Fh, 014h, 060h, 096h, 0b9h, 0abh, 0FFh

                 ; Attribute Controller offsets 00-13h
db 000h, 001h, 002h, 003h, 004h, 005h, 006h, 007h
db 008h, 009h, 00ah, 00bh, 00ch, 00dh, 00eh, 00Fh
db 001h, 000h, 003h, 000h

                 ; Graphics Controller offsets 00-08
db 000h, 000h, 000h, 000h, 000h, 020h, 005h, 00Fh, 0FFh

                 ; DAC Palette registers 0-3
db 000h, 000h, 000h                ;reg 0: black
db 01ah, 01ah, 01ah                ;reg 1: grey
db 01ah, 01ah, 01ah                ;reg 2: grey
db 02ah, 02ah, 02ah                ;reg 3: white

;*******************************************************************
LTABLE label byte  ; parameter table for 640*400 mode

db 000h, 000h, 000h, 000h, 000h    ; Dymmy header
db 011h, 00Fh, 000h, 00eh          ; Sequencer offsets 01-04
db 063h                            ; Miscellaneous register

                 ; CRT Controller offsets 00-18h
db 05Fh, 050h, 052h, 0e2h, 054h, 0e0h, 0bFh, 01Fh
db 000h, 000h, 000h, 000h, 000h, 000h, 000h, 000h
db 09ch, 00eh, 08Fh, 014h, 060h, 096h, 0b9h, 0a3h, 0FFh

                 ; Attribute Controller offsets 00-13h
db 000h, 001h, 002h, 003h, 004h, 005h, 006h, 007h
db 008h, 009h, 00ah, 00bh, 00ch, 00dh, 00eh, 00Fh
db 001h, 000h, 001h, 000h
                 ; Graphics Controller offsets 0-8
db 000h, 000h, 000h, 000h, 000h, 000h, 005h, 00Fh, 0FFh
                 ; DAC Palette registers 0-3
db 000h, 000h, 000h                ;reg 0: black
db 02ah, 02ah, 02ah                ;reg 1: white
db 02ah, 02ah, 02ah                ;reg 2: white
db 02ah, 02ah, 02ah                ;reg 3: white

SETMODE endp

;*******************************************************************
DRAWCHR proc near
; this procedure draws a character on the screen in the graphics
; mode; parameters are expected to be as follows:
; AL: -- char code
; BX: -- bit map width
; DX: -- font height (8 bits only)
; DS:SI -- Disp Mem pointer
; ES:DI -- Font pointer

        push    cx              ;save CX
        mov     cx,dx           ;get char height in CX
        mul     dl              ;AX gets font offset for character
        add     di,ax           ;ES:DI gets font address for font
LABLO:
        mov     ah,es:[di]      ;read font pattern
        mov     ds:[si],ah      ;write into display memory
        inc     di              ;next line of font pattern
        add     si,bx           ;next line in display memory
        loop    LABLO           ;repeat for every scan line
        pop     cx              ;retrieve CX
        ret
DRAWCHR endp

;*******************************************************************
W_INDEXREGS proc near
;This procedure reads a byte from the parameter table and then
;writes it to a index/data register.
; AH = index number of first register to receive parameter
```

```
; CX = # of index registers to be loaded
; DX -- I/O port address,
; DS:SI -- points to parameters

        lodsb                   ;load parameter from table into AL
        xchg    al, ah          ;get index in AL, data in AH
        out     dx, ax          ;write index/data register pair
        xchg    al, ah          ;get index in AH
        inc     ah              ;next index
        loop    W_IndexRegs     ;repeat
        ret
W_INDEXREGS endp

;*********************************************************************
W_ATTR_REGS proc near
;This procedure reads a byte from the parameter table and then
; writes it to a self index/data register.
; AH = index number of first register to receive parameter
; CX = # of index registers to be loaded
; DX -- I/O port address,
; DS:SI -- points to parameters

        xchg    al, ah          ;get index in AL
        out     dx, al          ;write index
        xchg    al, ah          ;get index in AH
        lodsb                   ;get data from table in AL
        out     dx, al          ;write data
        inc     ah              ;next index
        loop    W_Attr_Regs     ;repeat
        ret
W_ATTR_REGS endp

;*********************************************************************
W_PALETTE proc near
; This procedure reads a byte from the parameter table and then
; writes it to the G171 palette/DAC. DS:SI -- point to parameters,
; AH = starting index number,
; CX = # of index registers,
; DX -- I/O addr of DAC address reg,
; DS:SI pointer to data area

        mov     al,ah           ;get start index number
        out     dx,al           ;send it to address reg
        inc     dx              ;point to DAC data reg
W_pal1: lodsb                   ;load data parameter
        out     dx, al          ;write red data
        lodsb                   ;load next data byte
        out     dx, al          ;write green data
        lodsb                   ;repeat w/blue data
        out     dx, al
        loop    W_Pal1          ;repeat w/next palette reg
        ret
W_PALETTE endp

;*********************************************************************
RD_INDEXREG proc near
;This procedure reads an indexed VGA register
; Input: AL = index number of register
;        DX = I/O address of register
; Ouput: register contents returned in AL

        out     dx,al           ; write index
        inc     dx              ; point to data register
        in      al,dx           ; read data register
        dec     dx              ; point to index register
        ret
RD_INDEXREG endp

;*********************************************************************
VERT_SCROLL proc near
; This procedure scrolls the screen up or down by a specified number
; of lines; parameters are expected to be as follows:
;       AX -- scroll count, # scan lines in 2's complement form,
;             negative for scroll down
;       BX -- bit map width

        imul    bx              ;AX = bytes to scroll
        mov     bx,ax           ;save start address change in BX
        mov     dx,3d4h         ; CRT address
        mov     al,0ch          ; start address high
        call    Rd_IndexReg     ;read register
        mov     ah,al           ;move to AH
        mov     dx,3d4h         ; CRT address
        mov     al,0dh          ; start address low
        call    Rd_IndexReg     ;read register
        add     bx,ax           ;add change to old start address
        mov     ah,bh           ;to get new start address, write the
        mov     al,0ch          ;high byte back to CRTC
        out     dx,ax           ;write new start address (HIGH)
        inc     al              ;point to start address LOW register
        mov     ah,bl           ;get lower byte of start address
        out     dx,ax           ;write new start address (LOW)
        ret
VERT_SCROLL endp

;*********************************************************************
HORIZ_SCROLL_4 proc near
; This procedure scrolls the screen left or right by a specified
; number of pixels. Parameters are expected to be as follows:
;       AX -- scroll count, # pixels in 2's complement form,
;             positive - scroll right, negative, scroll left.

        mov     bx, ax          ;save scroll count
        mov     dx,3d4h         ; CRT address
        mov     al,0ch          ; start address high
        call    Rd_IndexReg     ;read register
        mov     ah,al           ;move to AH
        mov     dx,3d4h         ; CRT address
        mov     al,0dh          ; start address low
        call    Rd_IndexReg     ;read register
        mov     bp,ax           ;save current start address
        mov     dx,3d4h         ; CRT address
        mov     al,08h          ; byte panning control
        call    Rd_IndexReg     ;read register
        mov     cl,2
        shr     al,cl           ;divide by 4
        and     al,18h          ;retain bits D3 and D4 only
        mov     ah,al           ;save in ah
        mov     dx,3DAH         ;Status register address
        in      al,dx           ;reset attribute flip flop
        mov     dx,3C0H         ;address for attribute controller
        mov     al,33h          ;Panning Control
        out     dx,al           ;point to attribute panning register
        inc     dx              ;point to data register
        in      al,dx           ;read current byte panning control
        dec     dx              ;point back to Attr Ctrl address
        and     al,7            ;retain bits D0-D2
        add     ah,al           ;get old absolute panning control
        mov     al,ah           ;move to AL, 0 into AH
        xor     ah,ah           ;Absolute panning in AX
        add     bx,ax           ;compute new absolute panning
        mov     ax,bx           ;get it into AX
        and     al,7            ;retain bits D0-D2
        out     dx,al           ;write new attribute pan control
        mov     ax,bx           ;new absolute pan control in AX
        mov     cl,2
        shl     ax,cl           ;multiply by 4
        mov     ah,al           ;save in AH
        and     ah,60h          ;retain bits D6-D5
        mov     dx,3D4H         ;CRTC address
        mov     al,8            ;index for byte panning control reg
        out     dx,ax           ;write new byte panning control
        mov     cl,5
        sar     bx,cl           ;start address adjust
        add     bx,bp           ;new start address
        mov     ah,bh           ;upper bits go into start address
        mov     al,0ch          ;Start Address high register index
        out     dx,ax           ;Write start address high
        inc     al              ;Start Address low index
        mov     ah,bl           ;low byte of start address
        out     dx,ax           ;Write start address low
        ret
HORIZ_SCROLL_4 endp

EndOfProgram label byte
code    ends
        end
```

Listings can be downloaded using PCTECHline, 301/740-8383. Parameters: 2400/1200/300 bps, no parity, 8 data bits, 1 stop bit.



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- Help: System and context sensitive.
- Screens: Screen display, color palettes, save, restore, scroll, more.
- Windows: Exploding, tiled, pop-up, overlapping. Direct video access and virtual. Up to 50 active at any time.
- Keyboard Handling: Regular, function, interrupt, background procedures.
- Editing: String and word wrap text.
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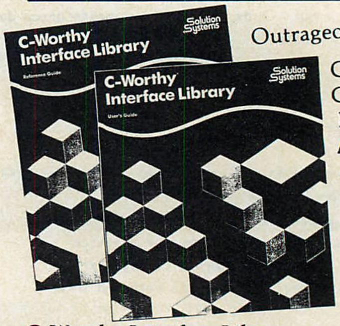

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OUTFITTING THE END USER

Desirements and Dreams

The task of clarifying a new system's requirements is unpopular at best, but failure to do so is invariably worse.

Two times in recent years I have been faced with every developer's nightmare: a client too important to be dismissed, bringing me a piece of code that even he does not fully understand, and asking me to perform major maintenance on the program.

In one case, a video game developer needed a PC*jr* version of a product for the Apple II. The only "documentation" available was the Apple II program and its assembly-language source code. That code contained exactly one comment: the original author's name and date.

The other case involved a program for cost estimation. The client wanted to add options for analyzing alternatives without reentering the unchanged portions of the input. The costing model that the program applied had been updated many times, but the only record of these modifications was the program itself. In this case also, comments were minimal; there even were some serious inconsistencies in the way that costs were calculated, not noticed until the code was carefully read.

In each case, the client had to pay me to reverse-engineer the program by reading the code and observing its runtime behavior. One of the most expensive aspects of such work is the time required to make judgment calls. Is a particular behavior a feature (to be preserved), a quirk (to be ignored if it could be done more easily in a different way), a compromise (to be done better if possible), or a bug (to be fixed or documented)?

These situations demonstrate the substantial cost of failure to describe requirements for software: to produce definitions external to the (presumably) working code. These requirements go beyond description of runtime behavior—they extend through the entire life cycle of the program, because software design is truly a case of "pay me now, or pay me later."

FROM THE TOP

One of the world's largest purchasers of software, the U. S. Department of Defense (DoD), offers an instructive approach to the problem of detailing a system's requirements. People often poke fun, or become genuinely angry, at the complex procedures that result in seemingly ridiculous costs for military hardware. In the area of software, however, the DoD standards provide a useful checklist for content, even if you don't want to deal with the DoD's many separate documents.

The process begins with a top-level document called the System Specification, which specifies requirements but is carefully written so as *not* to specify the solution. In fact, the most recent revision of the DoD's overall procedure deletes several items from this document; for example, processor-memory size and word size were deferred until later in the process.

The critical issue at this top-level requirements stage is to avoid what Kurt Motamedi, professor of organization theory at Pepperdine University's School of Business and Management, calls "aspirin statements" (the term comes from a hypothetical medical diagnosis, "The patient has failed to take aspirin"). Such a statement says nothing about the real problem, but rather recasts the situation as the failure to apply the preconceived solution.

PIECE NEGOTIATIONS

The System Specification leads to the System Design Document, which describes the design of the system in the context of the environments in which it will be used and maintained. It breaks the overall concept into identifiable pieces of hardware and software, as well as identifying what people will have to do to make it all work.

Identifying the user operations is especially important when designing desktop systems—precisely the cases in which these operations must be minimized. There is a big difference, for example, between a backup system that takes one minute per megabyte (but requires the user to swap media every two minutes) and one that takes three *times* as long (but can back up 40MB without user intervention).

I predict greater user acceptance for the second system, in spite of its "lower" performance, but a design document that fails to spell out user operations may mask such trade-offs until the wrong choice is cast in silicon.

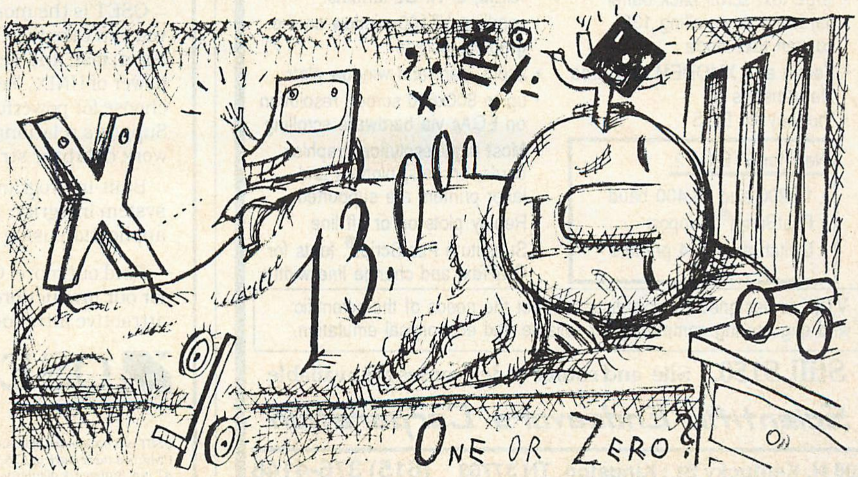

ILLUSTRATION • MACIEK ALBRECHT

Description of the use and maintenance environments is also important because it draws attention to the availability of help from other users (for software) and the availability of parts and supplies (for hardware). I have seen "alpha users" induce a department to select a word processor that was used by no other department in the company. "The whole company will be going to this one," they assured the manager. It hasn't happened, and the costs of being different have been real. These costs were never assessed up front because no equivalent of the System Design Document existed in the company's development process.

The same concerns hold for hardware: When you buy a printer, do you verify the availability of drivers for all your applications? When you buy a new computer, do you determine the types and sources of parts that will require replacement at regular intervals? I wonder, for example, how many buyers of the Macintosh II know that replacement of the clock/calendar battery is going to require unsoldering the old one from the system board.

Careful description of the environment also starts you thinking early about connectivity considerations; these are handled in the DoD procedure by an Interface Requirements Specification, which may deal with such details as the formats of data as well as the protocols for their transfer to and from external systems. You may not need to develop this as a separate document, but you need to cover this ground. What will your host connection be, if any? Are the required slots available? Be careful: some of the most exotic boards out there actually require an old-fashioned XT-style 8-bit slot, because their skirts come right up to the edge of that 8-bit connector. Details matter.

Ordinary peripheral interfaces are also a vital issue. For example, will you wind up needing three serial ports? It can be done on some systems, but will the applications accept the required port assignments?

Even if you do nothing more, this kind of environmental analysis can eliminate many of the unpleasant and expensive surprises that are associated with too many PC-based systems. If the system in question is nontrivial, however, consisting of more than a single turnkey item, you may want to go to the next level of detail—to negotiate, as it were, the same kind of understanding between the various pieces of the system that you have so carefully developed between the system and the rest of the world.

The DoD procedure spells out the responsibilities of each major piece of the system—each computer software configuration item (CSCI)—in a Software Requirements Specification (SRS). The SRS specifies which requirements from the top-level document have been "allocated" to a particular CSCI. The purpose of the document is not merely to give guidance to the developer, but (perhaps even more important) to spell out the criteria by which the customer will subsequently determine that the requirements have been met.

A private contractor, bd Systems of Torrance, California, in reviewing these DoD standards to determine their applicability to procurement of expert systems, has identified the following key criteria for a good SRS:

- Internal consistency
- Understandability
- Traceability to System Specification
- Consistency with the Interface Requirements Specification
- Appropriate allocation of resources such as size and time
- Adequate test coverage and testability of requirements

TESTS: ACID AND BASIC

That last item brings us to our Maxim of the Month: If it can't be tested, it isn't a requirement. Period. Call it a guideline, call it an indication of relative priority, but don't kid yourself that it's a requirement if you can't describe how you could prove that the system fails to meet it.

Consider the following: "The system shall permit rapid user development of new reports." What does this really mean? What we need, in order to test this statement, is a representative report format and description of how many keystrokes should be required to set up headers, footers, subheadings, column layout, and so on. (In deciding on a representative report format, you may even get a better handle on exactly what features you require—and how easy their use should be.)

Maybe you are not too worried about keystrokes but want to be sure that the user can at least figure out what to do. How about: "The system shall provide on-line help describing all steps required to develop a report using headers, footers, subtotals, and totals for a multicolumn format." Now there's a requirement that can be tested—but one that generates a completely different allocation of developer effort. You are going to pay for it, so you might as well get what you want.

Or perhaps I should say, "what your *users* want." Consider the following question, which I used to include on midterm exams. "A company hires a contractor to develop a new data-entry system with the goal of reducing user errors. The manager of the affected area meets with the contractor to define his requirements; the contractor produces a formal specification, which is reviewed and approved by the manager before actual programming begins. Is this a good example of the software development cycle?"

All but a few students messed up on this one. The ones who got it right noticed that nowhere in this scenario does the contractor talk to the users, the data-entry operators, the people who are making the errors that the manager wants to reduce. The manager may have no idea of the real problem with the existing system—even the operators may not recognize the cause. It takes someone on the scene—someone who understands users as well as understanding what they use.

Another item on the aforementioned list of criteria, the "traceability" of requirements to the top-level document, combines with my concern about understanding the user's real need, to make me a little bit nervous about the current fascination with computer-aided systems engineering (CASE) techniques. My apprehension is that CASE automates what is, in principle, the easy part of the job—the translation of a specification into executable code—while doing little to improve the likelihood that the result will be much closer to the user's actual needs.

By creating a whole new dimension of programmer performance, in the form of elaborate graphics, CASE provides one more distraction from the unpleasant task of getting away from the keyboard and out to the front lines. Instead of concentrating on the link between designer and programmer—as vital as that link is—we should be developing tools that improve the coupling between user and designer. We need tools that make it easier, for example, to forecast the consequences of user choices in terms of system cost and/or performance.

Traceability is important. Many managers are aghast to learn, months down the road, that their casual "wouldn't it be nice" remark in a long-forgotten meeting has been interpreted by a designer as an essential feature for a system that is (finally) nearing completion. If you document the origin of requirements, managers are more likely to say, "Wait! If I'm the only one who wants that, don't bother if it costs more than [fill in the blank]."

DEATH TO DESIREMENTS

The cost of a feature cannot be overlooked. I once sat in on a meeting that soon got to the heart of the matter: the budget for the work at hand. Someone rashly commented that a certain feature under discussion was a requirement, although the incremental funds had yet to be allocated for its development. The manager at the head of the table fixed him with a steely gaze and said, "Young man, there is no such thing as an unfunded requirement."

His point, I trust, is clear. It makes no sense to describe anything as required if you can't define what it's worth to you. When this has not been properly thought out, the proposal is a house of cards ready to collapse at the first disturbance. A term has been coined, I'm not sure by whom, for features that people would like to have but that they readily give up at the first hint of actual cost: *desirements.*

Many a frivolous proposal has been killed neatly by the polite but insistent question, "What will be the consequence of denying this request?" This is just a different slant on the question, "What's it worth to you?" If neither of these questions is part of your own in-house justification process for every kind of resource allocation—time, money, space, whatever—then there is a good chance that you are foregoing a powerful tool for the separation of signal from noise.

Be sure to recognize, too, that the consequence of concern may be a matter of common sense rather than dollars and cents. For example, in discussing the testability of requirements for a graphics system, a group of my clients had just about agreed that five seconds was an acceptable time limit for a zooming operation when a prospective user of the system spoke up from the back of the room: "Excuse me, but if it takes five seconds to do a zoom, I don't think I'll bother." Oops. We settled on a goal of half a second and a requirement of no more than two seconds, because this was one of the basic features that the system had to have—it had better be usably fast.

DON'T FORGET TO DOCUMENT

The DoD process includes two more vital documents: the Software User's Manual and the Software Programmer's Manual (SPM). User's manuals have been improved, in my opinion, by the recent trend toward dividing documentation into a tutorial manual and a reference manual; on-line help is also becoming better and more widely used, so I'll let well enough alone.

Too often omitted, however, is documentation of crucial matters such as file format—precisely the type of subject covered by the SPM—without which developing truly integrated systems can be extremely difficult. Note, for example, that Apple's much-vaunted HyperCard uses a file format that Apple refuses to disclose even to its so-called Certified Developers.

Some of these companies have reverse-engineered the format to develop utilities such as report generators, adding much-needed functionality to the program, but their work remains entirely vulnerable to future changes by Apple. I know at least one user who declared a boycott of all programs for which no file format is documented. If you also feel strongly about this, you might try a book called *More File Formats for Popular PC Software*, by Jeff Walden (John Wiley and Sons, 1987). Others have liked it.

OBJECTIONS TO OBJECTIVES

The problem with being the voice of reason is that it is never much fun to confront people with the weakness of their logic. This is particularly the case where computers are involved, because the typical user comes into the process with expectations so far in excess of reality that even the most gentle awakening is going to feel like falling out of bed—from the top bunk.

This is not the user's fault. Users can view a world where Captain Picard of the starship Enterprise can ask the computer a question, the computer can say "Insufficient data," and he can respond with the order: "Speculate!" Wouldn't *that* be nice.

Exposure to such possibilities leads to user requests that are not even desirements, but dreams. Expert systems are an example. People discuss them as if they were like the so-called

"smart cables" that automatically configure themselves based on the signals they see. Users ask if they can solve a problem with an expert system when all they really know about the problem is its symptoms.

The trick for us is to avoid being too much of a party pooper. We need to present the development process as one of helping the user get what he or she wants rather than as a procedural straitjacket. It's possible to talk about objectives as friendly aids to decision making. Arthur A. Thompson, Jr. and A.J. Strickland III, in *Strategic Management: Concepts and Cases* (Business Publications, Richard D. Irwin Inc., 1987), offer the following five-point list of criteria for a good objective. It should do the following:

- Relate to a single, specific topic
- Relate to a result, not an activity
- Be stated in measurable terms
- Contain a time deadline
- Be challenging but achievable

THE LONG, LONG VIEW

The expanding world of information is often compared to a vast uncharted ocean, with our increasingly powerful computers being the navigational tools that help us make the best use of its resources. With this image in mind, it's instructive to consider the remarks of Yale University history professor Paul Kennedy in his recent best-seller, *The Rise and Fall of the Great Powers* (Random House, 1987). Commenting on the relative level of advancement of the Far East, Europe, and the Islamic countries as maritime powers in the fifteenth century, he observes:

"There was little difference, one suspects, between all three regions in regard to cartography, astronomy, and the use of instruments like the compass, astrolabe, and quadrant. What was different was *sustained organization*: for example, the systematic collection of geographic data by the Portuguese."

In the same way, computers (like the compass and the astrolabe) are an enabling technology: a multiplier of intelligence and creativity, but not a substitute for either. Today and in the future, tools plus a well-considered strategy will triumph over the mastery of tools alone.

Peter C. Coffee is managing partner of SolveWare, a developer and business computing consultant, and is active in AI and distributed computing applications for aerospace and educational clients.

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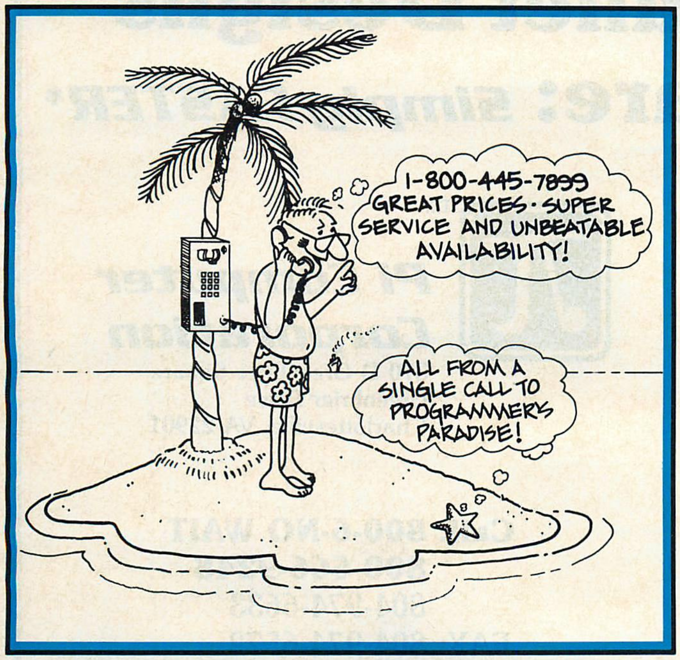

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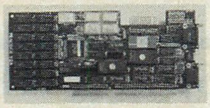

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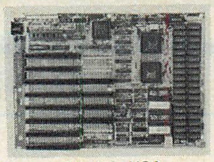

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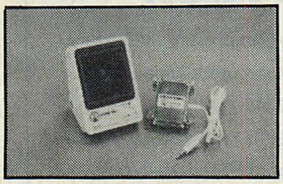

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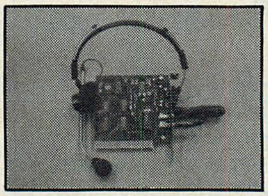

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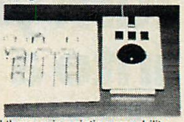

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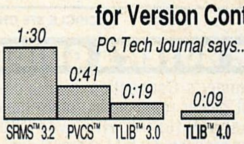

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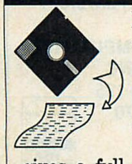

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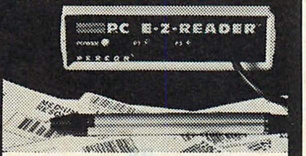

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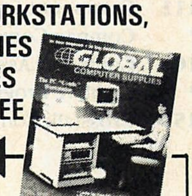

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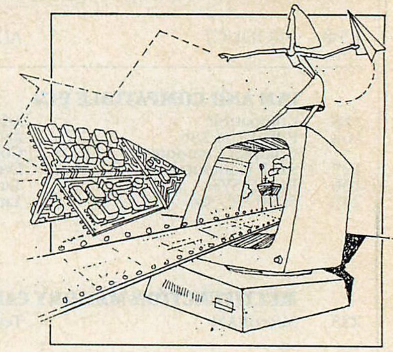


The focus is on prototyping, planning, and quick coding to streamline development, but tools vary considerably.

When you launch a software development project, does your experience resemble (a) "Lost In Space" or (b) a flight aboard the Concorde—smooth, fast, and focused?

The primary strategy to streamline systems development, say respondents to an informal *PC Tech Journal* reader opinion poll (August 1988), is to produce a prototype of the system and get feedback from users. Prototyping can identify potential problems, focus direction, and ensure happier users.

A second priority for streamlining systems development is good advance planning. (For more on systems planning, see "Outfitting the End User," Peter Coffee, this issue, p. 151.) Priority three, say respondents, is writing, editing, and compiling applications' code using faster tools.

When it comes to achieving these goals, the specific tools vary considerably. Most respondents have an arsenal that includes prototyping and computer-aided systems engineering (CASE) tools, debuggers, compilers, editors, and languages from various vendors.

Those developing systems for larger companies tend to use comprehensive CASE tools, while those building applications for smaller clients prefer to mix and match individual tools. Of CASE tools, Excelerator from Index Technology is mentioned most often; of prototyping tools, Dan Bricklin's Demo Program from Software Garden is most frequently singled out. Solution Systems' BRIEF editor and Microsoft's CodeView debugger are also popular.

Code generators, which automatically generate executable code from design specifications, are relatively immature in the PC market, but several respondents say they either use them or intend to. "I plan to purchase Matrix Layout [a screen generator from Matrix Software Technology Corporation]," says John Williams, president of XL Systems Inc. in Renton, Washington.

On a hardware note, computer specialist Jim Wheelock, of Prudential Insurance in Woodland Hills, California, speaks for several respondents, saying he uses "the fastest machines possible [so I can] spend time being creative, not waiting."

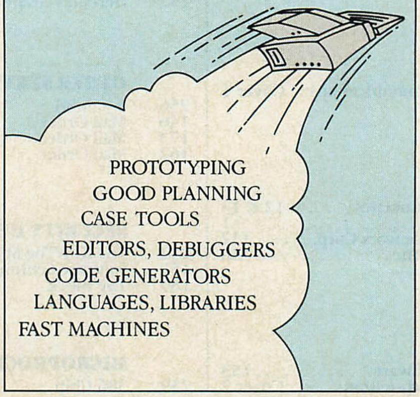
A MODEL SYSTEM

While it may seem that developing a prototype is time consuming, respondents agree that it actually *saves* time and, in the long run, money.

"Prototyping allows us to get feedback to see if we are on the right track. It removes the need for extensive design specifications, [resulting in] better systems and happier users," says programmer/analyst Dean Campbell of Salt Lake City Corporation in Utah.

Even beyond prototyping, respondents stress the need for continuous user interaction. Craig A. Richmond, manager of finance systems at Princeton University in New Jersey, says that "technical tools and methodologies aside, the real guts of design work is *communication*—users, managers, analysts, and programmers sitting down and discussing needs and concepts."

What tools or techniques do you use to streamline the systems development process?



PLANNING STRATEGIES

For most, advance planning means taking a structured approach to systems development, using data from the analysis phase in the design process, and standardizing modules so they can be reused. One in five respondents depends on CASE tools to automate structured planning and design. (For an overview of CASE tools, see "The CASE For Structured Development," Carma McClure, August 1988, p. 50.)

"Excelerator allows me to model requirements and system design in a simple project database," says Scott Whitmire, president of Advanced Systems Research, Ltd., Renton, Washington. "Using the same data in analysis and design saves time and promotes consistency."

"I automate every step so I can concentrate on design and debugging rather than on remembering the development steps. I use batch files, MAKE files, DOS enhancement tools, editor macros, and so on," says Robert Kircher, process engineer, Willamina Lumber Company, Portland, Oregon.

Todd Fritsche, manager of research and development, Foodcom Inc., Malvern, Pennsylvania, says, "We make significant aspects of an application (such as file maintenance and screen I/O) modular, maintaining a high level of interprocess communications among modules. Fourth-generation language (4GL) systems make design and integration of these modules easier."

THE EAGLE HAS LANDED

Respondents are looking for ways to plan better, to get user input more frequently, and to prototype faster. They want quick development languages, such as 4GLs, and fast, fully functional editors, compilers, and debuggers to speed coding and debugging. Many are also starting to look at code generators, indicating that potential market growth is high for these tools.

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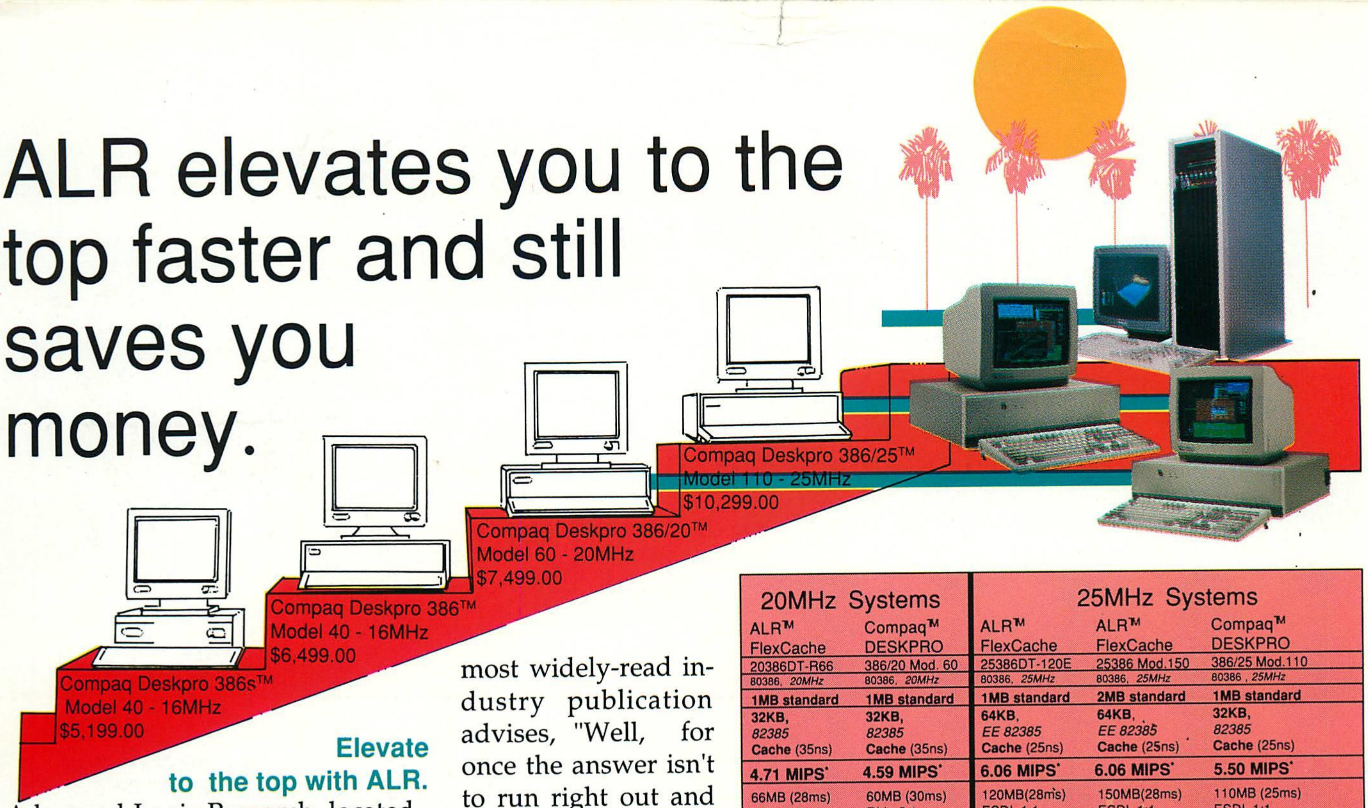

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-First Looks , March 15, 1988 -

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